PIC16F630/676

PIC16F630/676 Rev. A Silicon/Data Sheet Errata

The PIC16F630/676 parts you have received conform functionally to the Device Data Sheet (DS40039**E**), except for the anomalies described below.

All issues listed here will be addressed in future revisions of the **PIC16F630/676 silicon**.

1. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer Interrupt Service Routine to verify the EEPROM write success.
4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

2. Module: Power-on Reset (Rising V_{DD} Detect)

The PIC16F630/676 Power-on Reset (POR) circuitry is sensitive to a low V_{DD} level and may fail to release the Reset if V_{DD} returns to an operational voltage after dropping to a very low level.

The sensitive V_{DD} condition occurs when V_{DD} drops into an out-of-specification voltage region below the Brown-out Detect threshold and then recovers to a normal operating condition. The voltage region that can cause the problem is dependant upon temperature with the region growing as the temperature drops. A typical region is between 0.5 and 0.7V at -25°C. Below the region, the POR operates correctly. Above the region, the POR is inactive per the data sheet. Inside the region, the POR will assert Reset and will not release Reset until power is removed and V_{DD} reaches V_{SS}. Because the POR is independent of other Reset circuits (see Figure 9-4 of the data sheet), activating BOR or using the MCLR input will not eliminate the problem.

Work around

To resolve this problem the application must be designed to assure that V_{DD} reaches V_{SS}. This is described as D003 V_{POR} in **Section 12.0 "Electrical Specifications"** in the Device Data Sheet (DS40039).

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40039**E**), the following clarifications and corrections should be noted.

1. Module: Product Identification System

In the Product Identification System description, the package “SOIC (Gull wing, 3.90 mm body) lists the package code as **SN**. The correct package code for this device is **SL**. “Example b” should read I/**SL**, as shown in bold print in Figure 1 below.

FIGURE 1: PRODUCT IDENTIFICATION SYSTEM

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC16F6XX:	Standard V_{DD} range 2.0V to 5.5V
	PIC16F6XXT	V_{DD} range 2.0V to 5.5V (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	P =	PDIP
	SL =	SOIC (Gull Wing, 3.90 mm body)
	ST =	TSSOP (4.4mm)
Pattern:	3-Digit Pattern Code for QTP (blank otherwise).	

Examples:

a) PIC16F630 - E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301.

b) PIC16F676 - I/**SL** = Industrial Temp., SOIC package, 20 MHz.

2. Module: TRISA – PORTA Tri-state Register

Register 3-2: Correction to replace R/W-**x** with R/W-**1** as shown in bold.

REGISTER 3-2: TRISA – PORTA TRI-STATE REGISTER (ADDRESS: 85h)

U-0	U-0	R/W-**1**	R/W-**1**	R-1	R/W-**1**	R/W-**1**	R/W-**1**
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

bit 7-6: **Unimplemented**: Read as '0'

bit 5-0: **TRISA<5:0>**: PORTA Tri-State Control bit

1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note: TRISA<3> always reads 1.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3. Module: ANSEL – Analog Select Register

The ANSEL register address is 91h. Change all ANSEL register addresses called out as 9Fh to 91h in the following sections, as shown in bold:

In Section 3.1, PORTA and the TRISA Registers, in the note box:

Note: The ANSEL (**91h**) and CMCON (19h).....

In Section 3.3, PORTC, in the note box:

Note: The ANSEL register (**91h**) must be.....

In Section 4.3, Using Timer0 with an External Clock, in the note box:

Note: The ANSEL (**91h**) and CMCON (19h).....

In Section 5.4, Timer1 Operation in Asynchronous Counter Mode, in the note box:

Note: The ANSEL (**91h**) and CMCON (19h).....

In Section 9.4.1, RA2/INT Interrupt, in the note box:

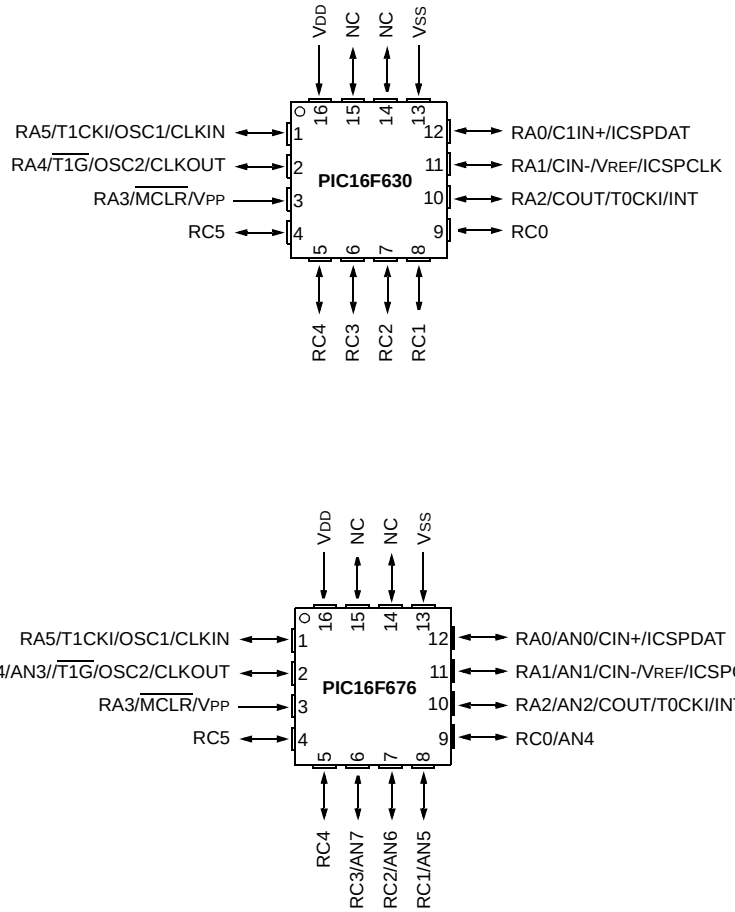
Note: The ANSEL (**91h**) and CMCON (19h).....

4. Module: New 4x4 QFN Package Added

The new 16-pin 4x4 QFN pinout diagrams will be added to the Pin Diagrams figure on page 2 and the Packaging Information chapter as shown below:

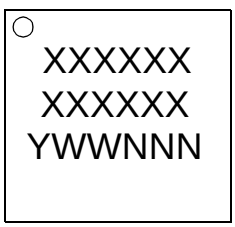
Pin Diagram

16-pin QFN

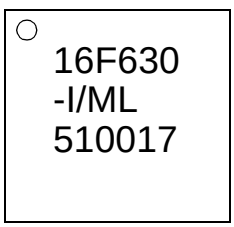


14.1 Package Marking Information

16-Lead QFN

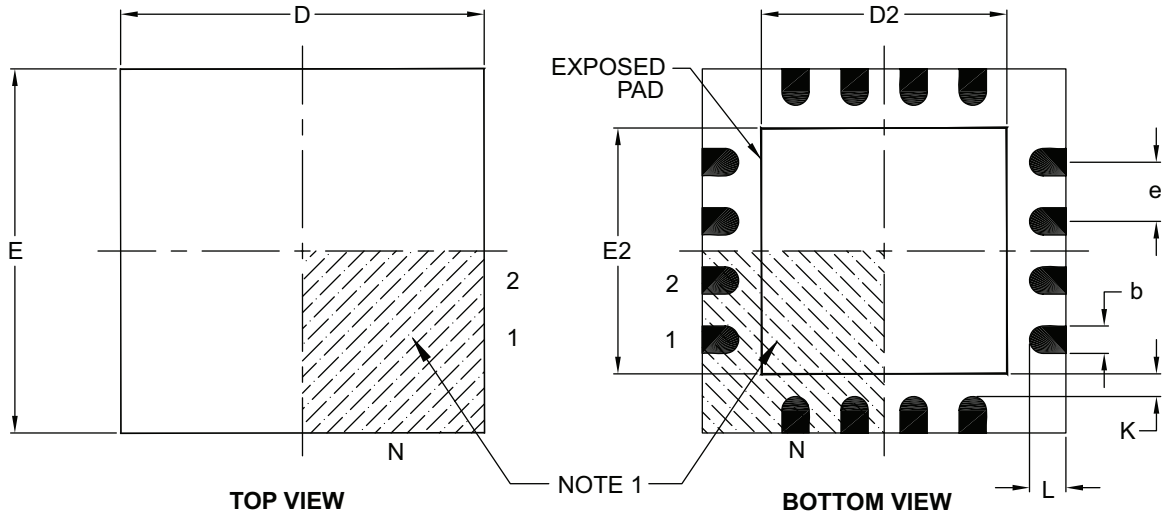


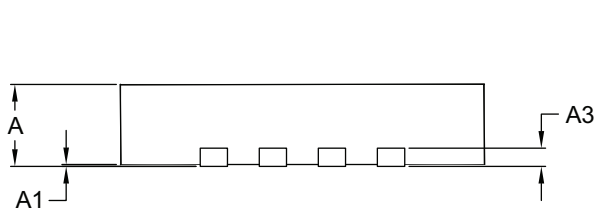
Example

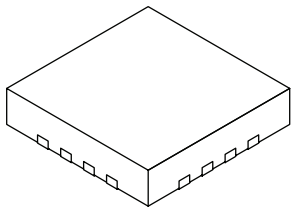


16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

5. Module: PORTA: Initializing Example

Change Example 3-1: Initializing PORTA to the following (bold text):

EXAMPLE 3-1: INITIALIZING PORTA

```
BCF     STATUS,RP0    ;Bank 0
CLRF    PORTA         ;Init PORTA
MOVLW   07h           ;Set RA<2:0> to
MOVWF   CMCON         ;digital I/O
BSF     STATUS,RP0    ;Bank 1
CLRF    ANSEL         ;digital I/O
MOVLW   0Ch           ;Set RA<3:2> as inputs
MOVWF   TRISA         ;and set RA<5:4,1:0>
                      ;as outputs
BCF     STATUS,RP0    ;Bank 0
```

APPENDIX A: REVISION HISTORY

Rev. A Document (04/02/04)

First revision of this document.

Rev. B Document (06/03/04)

Added Item 3, changing the ANSEL register address references from 9Fh to the correct address of 91h.

Rev. C Document (11/2004)

Added Module 1: “Data EEPROM Memory” for PIC16F630/676 silicon.

Rev D Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 4: New 4x4 QFN Package added.

Rev. E Document (8/2006)

Added Module 2: “Power-on Reset (Rising V_{DD} Detect)” for PIC16F630/676 silicon.

Rev. F Document (3/2007)

Data Sheet Clarifications/Corrections Section: Module 1, Figure 1 - updated package SL; Module 4 - updated QFN package; Added Module 5: “PORTA: Initializing Example” in the Data Sheet correction section.

NOTES:

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