Application Note: AS8506-AN02 – Passive Balancer

AS8506

AN02 – Passive Balancer

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Revision History

Revision	Date	Owner	Description
1.0	07.10.2013	gheh	Initial release

1 General Description

This document describes the AS8506 Passive Balancer Demo.

This kit demonstrates the AS8506 in conjunction with a host controller. Each board allows the balancing of up to 7 cells and multiple boards can be connected to support higher cell counts.

The hardware will support li-based cell packs as well as EDLCs.

Number of cells, target voltage as well as over and under voltage can be configured via a GUI

1.1 Kit Content

The kit consists of one double layer board with an 8 pin battery connector two stack connectors and a mini HDMI port to interface to the host controller and a mini-HDMI to micro-HDMI cable.

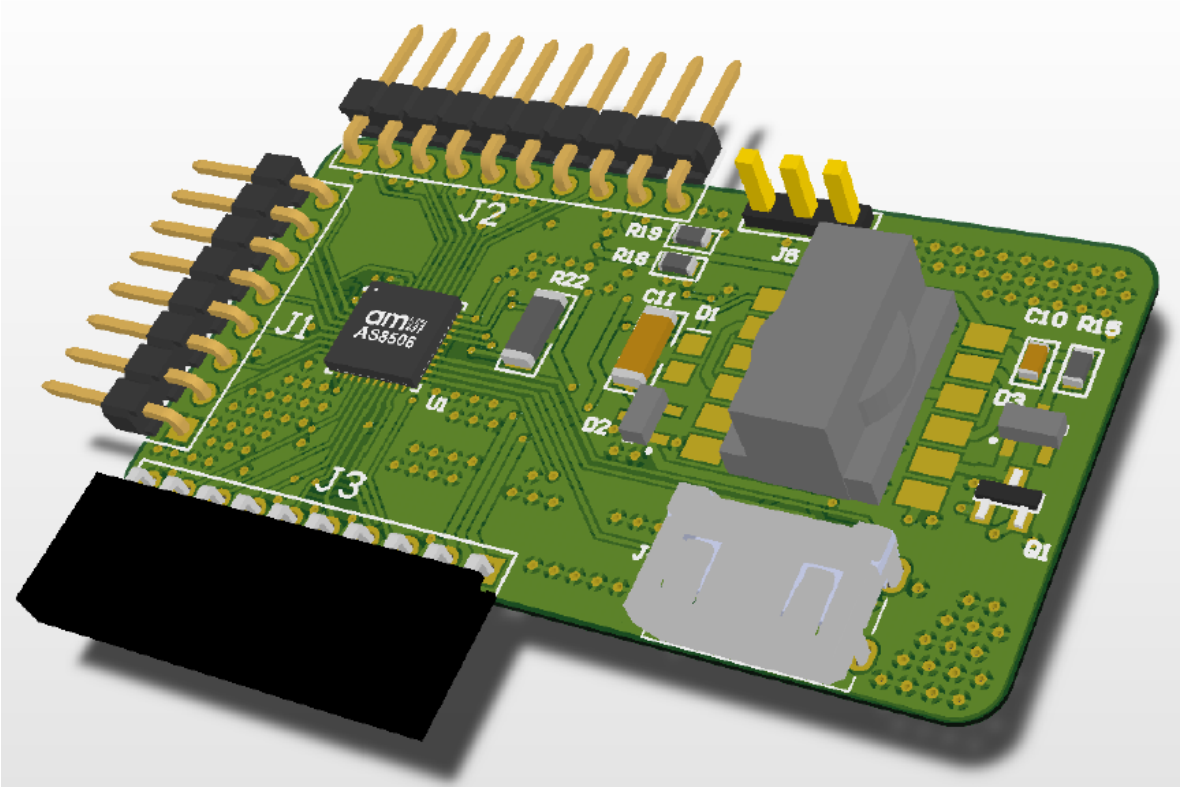

Figure 1: AS8506 Passive Board

2 Getting Started

To get started configure the device to your cell count and voltage specifications as described in chapter 4.

Also if you plan to connect multiple boards in a stack configure them as described in Section 4.3.

After having set up the hardware install the software that can be downloaded from:
www.ams.com/DK-Passive-Board

Once finished with the installation connect the batteries to the boards, connect the master board via the provided HDMI cable to the USB Interface board and connect that to a PC via USB. Now fire up the PC GUI.

You should be all set to explore the possibilities of the chipset via the GUI interface. As described in Section 5

3 Hardware Description

The AS8506 Passive demo is powered via the battery connected via J1. Unconnected pins (in case lower cell counts then 7 are used) are shorted out by the bridging resistor and can be left unconnected.

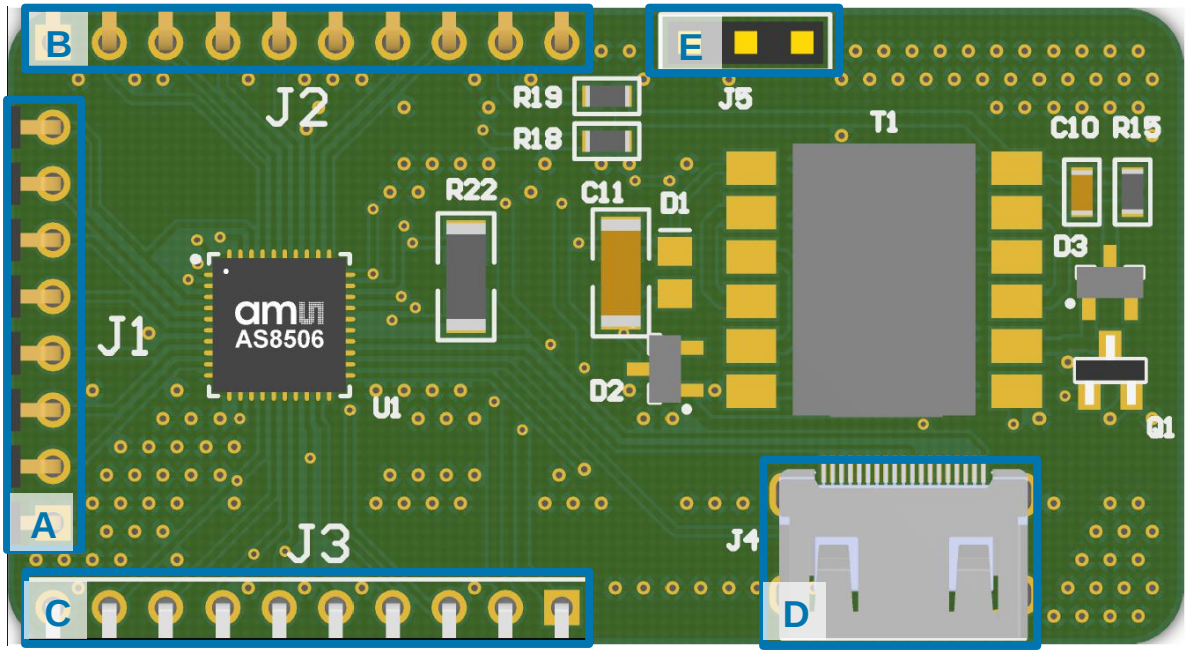

Figure 2: PCB Top Side Diagram

Label	Name	Designator	Description	Info
A	BATT	J1	Battery Connector	Connects to 3 to 7 cells GND on the bottom
B	TOP_CONN	J2	Top Connection	To stack multiple boards
C	BOT_CONN	J3	Bottom Connection	To stack multiple boards
D	AMS_HDMI	J4	Master Connection	Connects to the USB Interface Board via provided cable
E	TEMP	J5	Temp Sensor	Can be connected to external temp sensor

Table 1: Connection Diagram

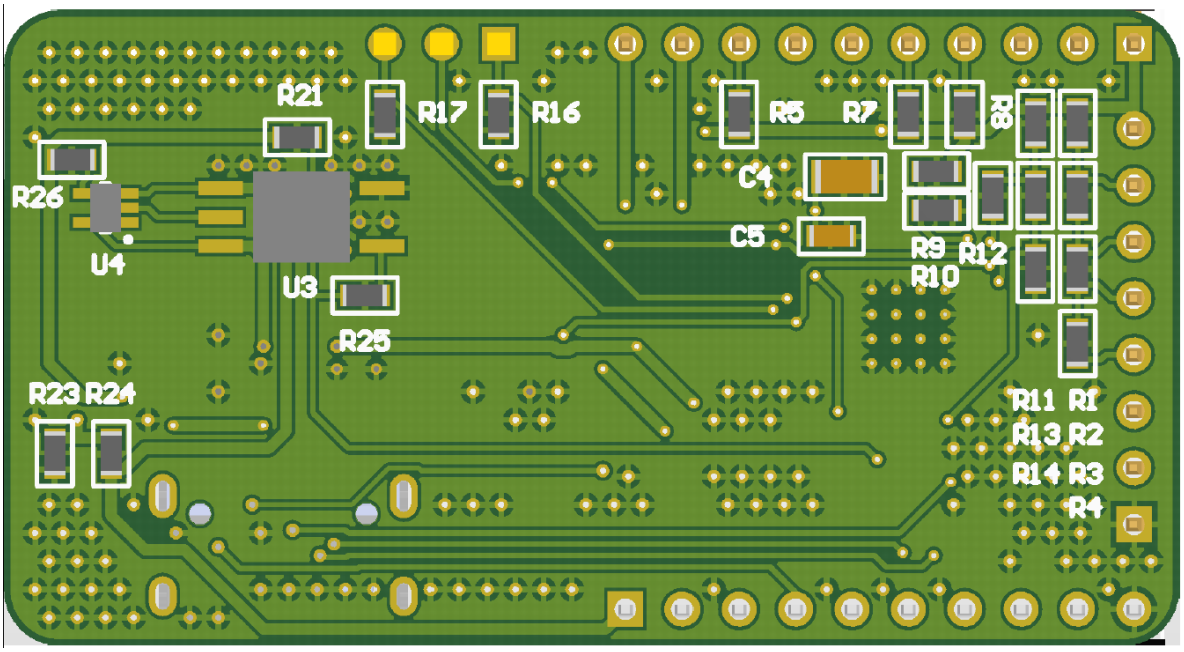

Figure 3: PCB Bottom Side Diagram

4 Configuration

4.1 Number of cells

Minimum number of cells to be balanced is 3 or as many to reach a battery voltage of at least 6V (cell chemistry / technology dependent). A maximum of 7 cells can be balanced by this board!

Remove zero ohm resistors according to table:

Cell-Nr	Remove
3	none
4	R4
5	R4, R3
6	R4, R3, R2
7	R4, R3, R2, R1

Table 2: Cell Adjust

4.2 Configuration of VREF

There are two options to set the balancing target voltage:

1. Defined by DAC via the GUI configuration interface
2. Defined by external voltage divider (has to be activated in the GUI)

   In case the second option is chosen or if you want to switch between the options the divider R13, R14 needs to be selected according to number of cells according to the following table:

Cell-Nr	R14	R13
3	100K	200K
4	100K	300K
5	30K	120K
6	150K	750K
7	20K	120K

Table 3: VREF relative adjust

4.3 Configuration of master/slave

If you want to chain multiple devices you have to configure the chained devices into slave mode and unsolder the stack termination registers from all but the topmost board

Multiple devices can be connected via J2 and J3 which just plug together.

The lowest board always has to be the master. Meaning this board has to be configured as master (which is the factory setting) and this board is the one to connect to the USB Interface box.

To configure a board for slave mode you have to move the 0Ω Resistor R10 to R9.

Then you have to unsolder R5, R7 and R8 termination resistors from all but the topmost board.

5 Software Description

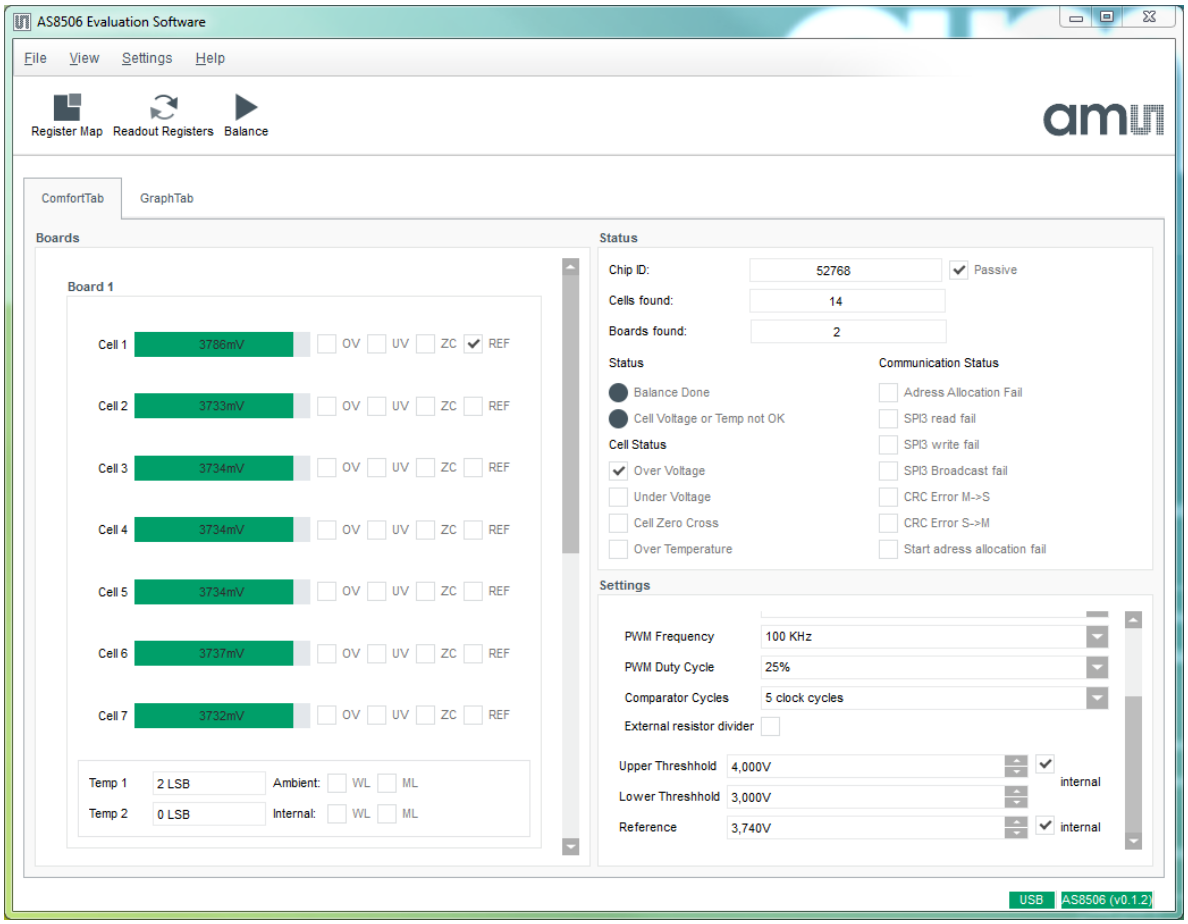

Figure 4: AS8506 GUI

Once started the PC GUI will automatically detect the AS8506 Boards connected to the USB Interface and enumerate those. The number of Cells will be displayed under “Cells found” and the number of Boards under “Boards found”

The GUI allows you to configure all settings of the AS8506 Chip.

The configuration can be either done via practical dropdown menus on the right-hand side in the ***Settings*** section or directly to the registers by clicking on ***Register Map*** and manipulating the registers in a bitwise fashion.

The settings should be pretty self-explanatory but keep in mind to set the correct lower and upper thresholds and reference if you’re using the DAC and activate the internal reference and thresholds in the checkboxes to the right:

Figure 5: Reference and threshold setting

All status information from the boards can by dynamically updated by activating the ***Automatic Update*** Feature under ***Settings***.

This will update ADC values as well as Over-voltage Under-voltage, Zero-cross, and Reference Status Information of each board connected every 2 seconds.

Once the balance process is started update rate will drop to every minute because the chip has to stop its balancing cycle to update the ADC and that should not happen too often.

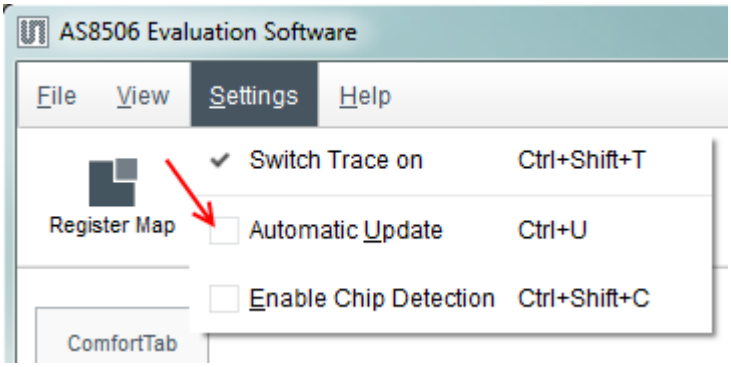

Figure 6: Automatic Update Feature

Also the ***Enable Chip Detection*** checkbox allows you to detect when AS8506 Boards have been unplugged from the Interface and reconnected.

Last but not least the 

Button allows you to activate the balance feature at will. Green button means balance is active. Gray means not active.

Balance Done LED will light green as soon as the balance process has finished and Cell Voltage or Temp not OK Led will light if the batteries exceed the set boundary limits.

In addition to this Tab there is a graphing tab which gives a graphical representation of the cell voltages and allows you to log the measured voltages to a file.

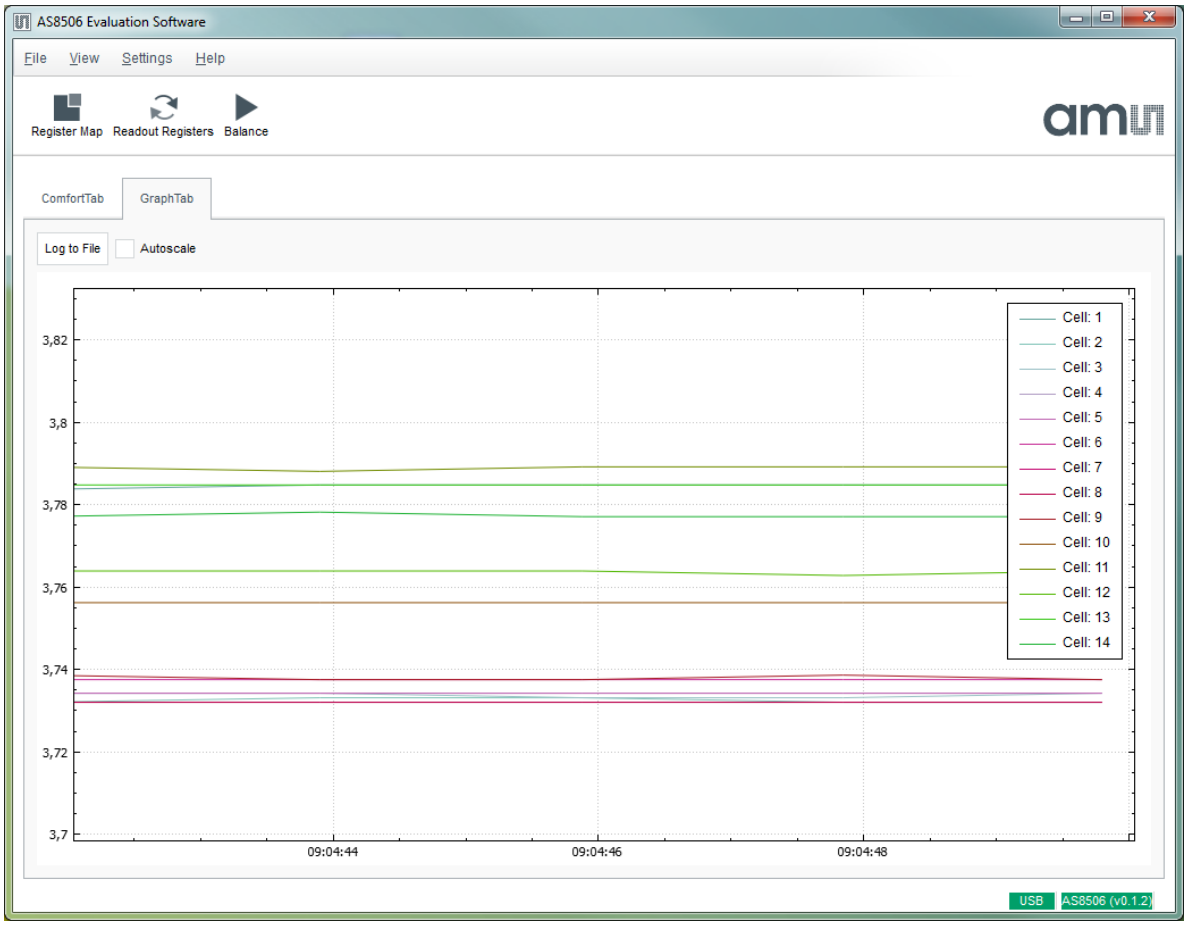

Figure 7: Graphing Tab

The ***Log to File*** button will open a file dialog which selects where the .csv log file will be saved.

From then on data that is acquired via the auto update function will automatically be logged to that file.

The ***Autoscale*** checkbox will automatically zoom in on the cell data. Also the window can be zoomed with the mouse wheel and moved with the left mouse button.

6 Board Schematics, Layout and BOM

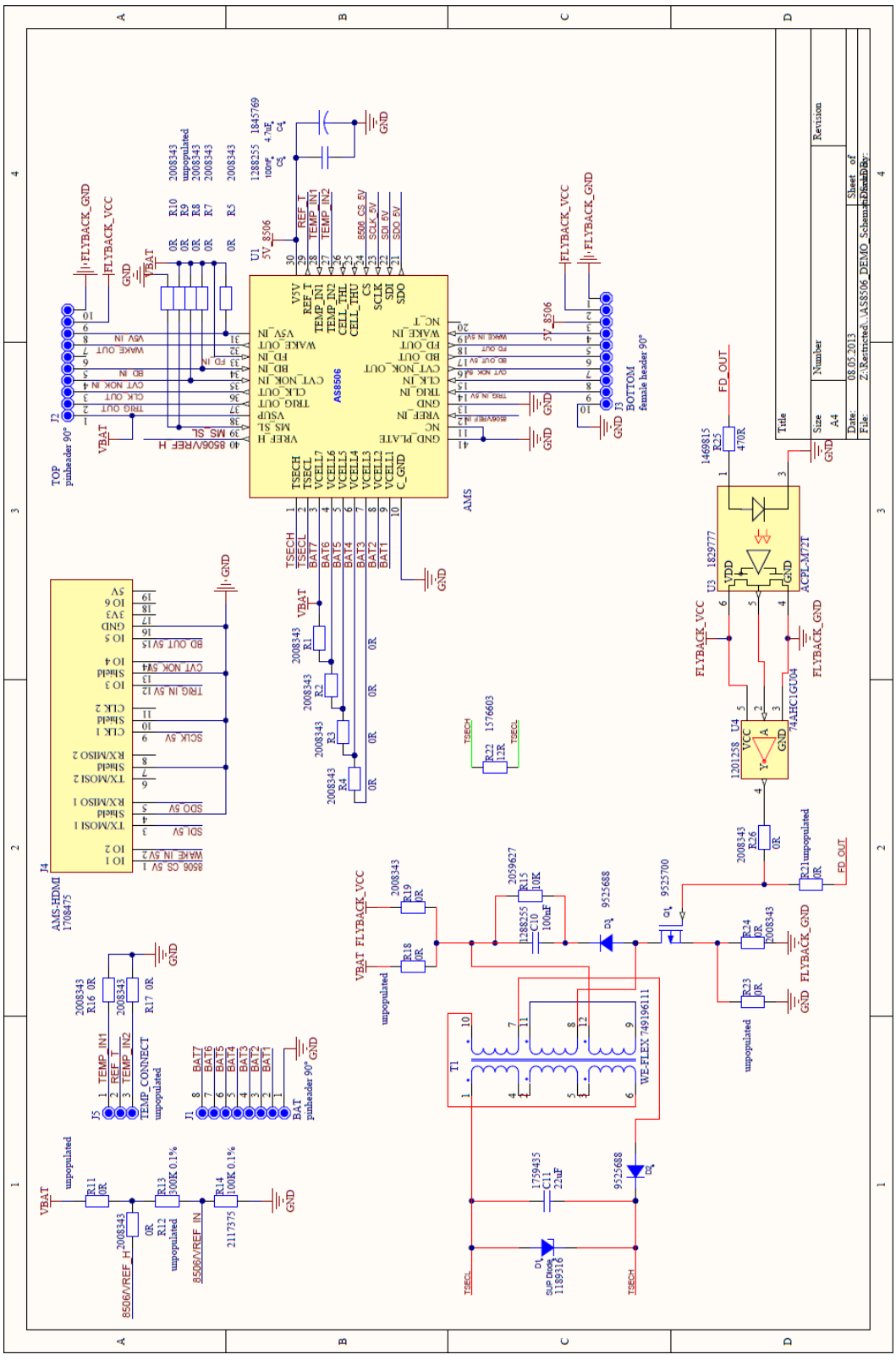

Figure 8: Schematic

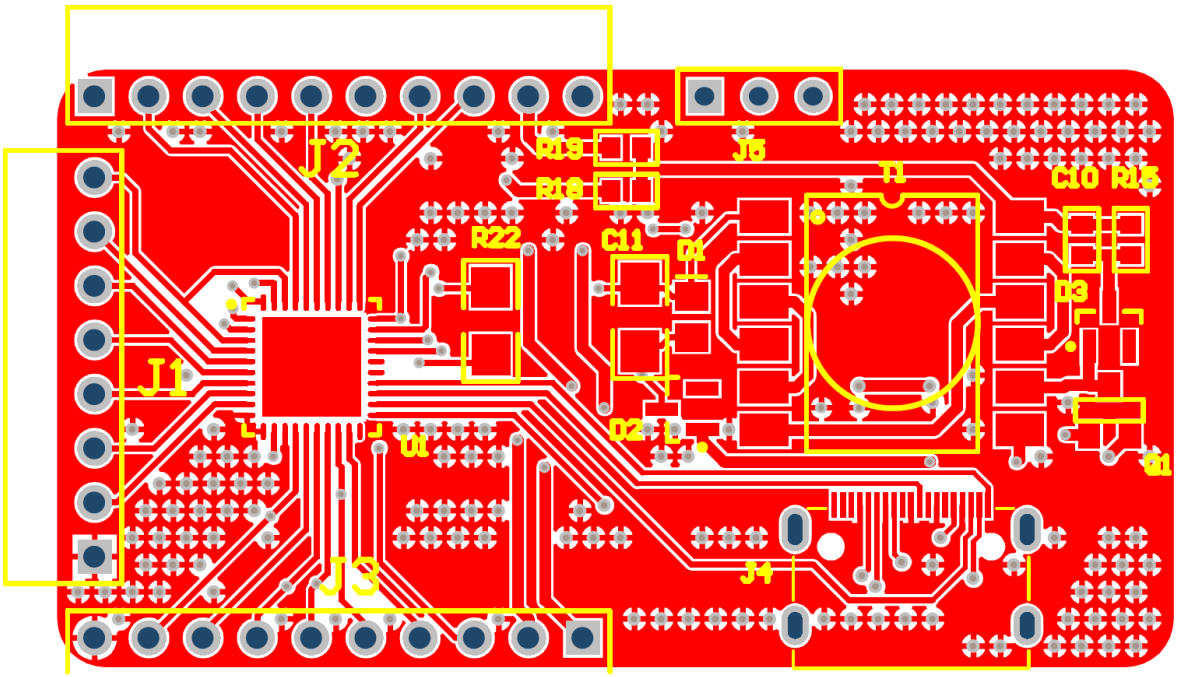

Figure 9: Top Layer

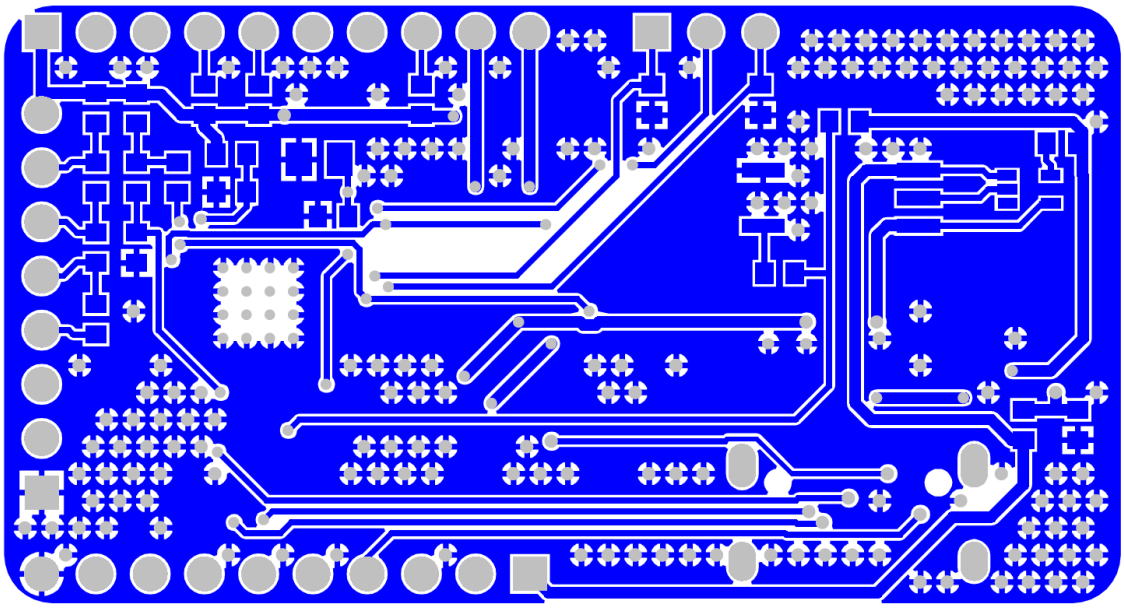

Figure 10: Bottom Layer

Bill of Materials

AS8506 Demo

Company:	ams AG
Originator:	GHEH
PCB Name:	AS8506 Demo
PCB Version:	0.4
Report Date:	12.12.2012

#	Designator	Comment	lame Error:Component_I	Manufacturer	Manufacturer Part Number	Quantity
1	C4	4.7uF		MURATA	GRM21BR71A475KA73L	1
2	C5	100nF		KEMET	C0603C104K5RACTU	1
3	C10	100nF		KEMET	C0603C104K5RACTU	1
4	C11	22uF		MULTICOMP	MCCA000555	1
5	D1	SUP Diode		AVX	VC080514A300DP	1
6	D2	ZLLS1000TA		DIODES INC.	ZLLS1000	1
7	D3	ZLLS1000TA		DIODES INC.	ZLLS1000	1
8	J1	BAT				1
9	J2	TOP				1
10	J3	BOTTOM				1
11	J4	AMS-HDMI		MULTICOMP	60U019S-341N-B1-FEC	1
12	J5	TEMP_CONNECT				1
13	Q1	ZXMN10A07F		DIODES INC.	ZXMN10A07F	1
14	R1	0R		BOURNS	CR0603-J/-000ELF	1
15	R2	0R		BOURNS	CR0603-J/-000ELF	1
16	R3	0R		BOURNS	CR0603-J/-000ELF	1
17	R4	0R		BOURNS	CR0603-J/-000ELF	1
18	R5	0R		BOURNS	CR0603-J/-000ELF	1
19	R7	0R		BOURNS	CR0603-J/-000ELF	1
20	R8	0R		BOURNS	CR0603-J/-000ELF	1
21	R9	0R				1
22	R10	0R		BOURNS	CR0603-J/-000ELF	1
23	R11	0R				1
24	R12	0R		BOURNS	CR0603-J/-000ELF	1
25	R13	300K 0.1%				1
26	R14	100K 0.1%		TE CONNECTIVITY	RP73PF2A100KBTDF	1
27	R15	10K		PANASONIC	ERJ3GEYJ103V	1
28	R16	0R		BOURNS	CR0603-J/-000ELF	1
29	R17	0R		BOURNS	CR0603-J/-000ELF	1
30	R18	0R				1
31	R19	0R		BOURNS	CR0603-J/-000ELF	1
32	R21	0R				1
33	R22	12R		MULTICOMP	MCHP06W2F120JT5E	1
34	R23	0R				1
35	R24	0R		BOURNS	CR0603-J/-000ELF	1
36	R25	470R		VISHAY DRALORIC	CRCW0603470RFKEA	1
37	R26	0R		BOURNS	CR0603-J/-000ELF	1
38	T1	WE-FLEX 749196111				1
39	U1	AS8506				1
40	U3	ACPL-M72T		AVAGO TECHNOLOGIES	ACPL-M72T-000E	1
41	U4	74AHC1GU04		NXP	74AHC1GU04GW/T1	1
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Figure 11: BOM

7 Ordering Information

The AS8605 Passive Balancer demo can be ordered via:

Table 4: Ordering Information

Ordering Code	Productname	Materialnumber
AS8506-DK-PASSIVE	AS8506 Passive Balancer Board	990600767

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