Dual IF Digital Variable Gain Amplifier **10 – 500 MHz IDTF1241NBGI**

General Description

The IDTF1241 (1 dB steps) is an IF VGA for Diversity Basestation receivers. The device offers significantly better Noise and Distortion performance than currently available devices. It is packaged in a compact 5x5 Thin QFN with 200 ohm differential input and output impedances for ease of integration into the receiver lineup.

Competitive Advantage

The IDTF1241 IF VGA improves system Signal-to-Noise Ratio (SNR), especially at lower gain settings. Via IDT's proprietary FlatNoise™ technology both $IP3_O$ & NF are kept virtually flat while gain is backed off, enhancing SNR significantly under high level interferer conditions, and greatly benefiting 2G/3G/4G Multi-Carrier IF sampling receivers.

The fast-settling gain step of 1 dB coupled with pinpoint accuracy allow for SNR to be maximized further by targeting the minimum necessary gain in small, accurate increments.

See the 'Applications Information' section starting on Page 17 for more details of the benefits of the F1241 in IF sampling receivers.

Part# Matrix

Part#	Range / Step	$IP3_O$	IF freq range	NF	Pinout Compatibility
F1241	20 to -11 1.0	48	10 - 500	4	ADI
F1240	20 to -11.5 0.5	47	10 - 500	4	TI (NSM)

Ordering Information

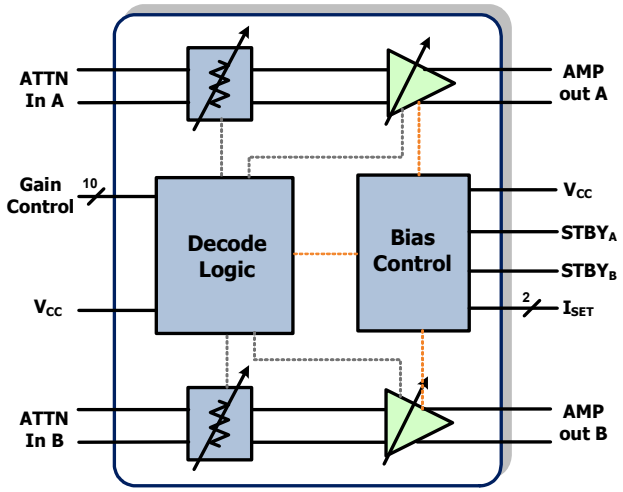
Features

- Ideal for systems with high SNR requirements
- 20 dB typical Maximum Gain
- 5-bit, 1 dB step, 31 dB gain control range
- Excellent Noise Figure = 4.0 dB
- 5mm x 5mm 32 pin package
- **200** Ω Differential Matched Input
- **200** Ω Differential Matched Output
- No termination resistors required
- NF degrades just 1.3 dB @ 10 dB below Max Gain
- 10 MHz – 500 MHz frequency range
- Ultra-Linear: $IP3_O$ +48 dBm typical
- Excellent 2nd Harmonic Rejection < -80 dBc
- Parallel Control
- External current setting resistors
- Very fast settling < 15 nsec
- Individual Power Down Modes
- Extremely Low Power: 80 mA / Chan

Applications

- Base Station 2G, 3G, 4G, TDD radiocards
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios

Device Block Diagram



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.3V to +5.5V
GA[5:1], GB[5:1], $STBY_A$, $STBY_B$	-0.3V to (VCC_ + 0.25V)
OUT_A-, OUT_A+, OUT_B-, OUT_B+	-0.3V to (VCC_ + 0.25V)
IN_A-, IN_A+, IN_B-, IN_B+	-0.3V to +2.2V
ISET_A, ISET_B to GND	-0.3V to +2.2V
RF Input Power (IN_A-, IN_A+, IN_B-, IN_B+) @ G_{MAX}	+15 dBm
Continuous Power Dissipation	1.5W
θ_{JA} (Junction – Ambient)	+40°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +100°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s) .	+260°C

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

TRUTH TABLE

Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name
20	00000	G_{20}	9	01010	G_9	-2	10110	G_{-2}
19	00001	G_{19}	8	01011	G_8	-3	10111	G_{-3}
18	00010	G_{18}	7	01100	G_7	-4	11000	G_{-4}
17	00011	G_{17}	6	01101	G_6	-5	11001	G_{-5}
16	00100	G_{16}	5	01110	G_5	-6	11010	G_{-6}
15	00101	G_{15}	4	01111	G_4	-7	11011	G_{-7}
14	00110	G_{14}	3	10000	G_3	-8	11100	G_{-8}
13	00111	G_{13}	2	10001	G_2	-9	11101	G_{-9}
12	01000	G_{12}	1	10010	G_1	-10	11110	G_{-10}
11	01001	G_{11}	0	10011	G_0	-11	11111	G_{-11}
10	01010	G_{10}	-1	10100	G_{-1}			

IDTF1241 SPECIFICATION

Specified values apply at V_{CC} = +5.0V, **f_{RF} = 200MHz**, T_C= +25°C, $STBY_A$, $STBY_B$ = 3.3V or NC, **R37 & R38 = 3.83K** unless otherwise noted. EVkit transformer losses are de-embedded

Parameter	Comment	Symbol	min	typ	max	units
Logic Input High		**V_{IH}**	2.0			V
Logic Input Low		**V_{IL}**	0		0.8	V
Logic Current	GA[5:1], GB[5:1] V_{IH} = 3.45 V, V_{IL} = 0V	**I_{IH}, I_{IL}**	***-2***		***+2***	µA
Logic Current[3]	V_{MODE}, STBY_A, STBY_B V_{IH} = 3.45 V, V_{IL} = 0V	**I_{IH}, I_{IL}**	***-10***		***+1***	µA
Temperature	Operating Case Temp Range	**T_{CASE}**		-40 to 100		degC
Voltage	All Supplies Operating Range	**V_{CC}**	4.75	5.00	5.25	V
Supply Current	Total, All V_{CC}	**I_{SUPP}**		***159***	***176***[1]	mA
Standby Current	Total, All V_{CC} ▪ STBY_A, STBY_B < V_{IL}	**I_{STBY}**		***2***	***5***	mA
Frequency Range	Low Distortion Range ▪ IP3O > 40 dBm, Pout +3 dBm/Tone ▪ Gain Set = G_{20}	**f_{RF}**		50 to 400		MHz
Frequency Range	Operating Range ▪ Gain > 17 dB ▪ With L1,L2,L3,L4 = 1500 nH	**f_{RF}**		5 to 560		MHz
1dB Gain Rolloff	Frequency @ 1dB Gain reduction vs. 100 MHz Gain	**BW**		400		MHz
Input Resistance[4]	Differential (> 10 dB RL)	**R_{IN}**		200		Ω
Output Resistance[4]	Differential (> 15 dB RL)	**R_{OUT}**		200		Ω
Maximum Gain		**G_{20} or G_{MAX}**	***18***	***20.2***		dB
Minimum Gain		**G_{-11} or G_{MIN}**		***-10.8***	***-9***	dB
Minimum Gain Step	Least Significant Bit	**LSB**		1.0		dB
Phase Error	Maximum phase change between G_{MAX} and any state down to G_{-4}	**IPE**		3		deg
Differential Gain Error	Between any two adjacent 1 dB steps	**DNL**		0.03		dB
Integral Gain Error	Error vs. line (G_{20} Ref)	**INL**		0.04		dB
Noise Figure	At G_{20}	**NF**		4.0	4.5[2]	dB
Noise Figure	At Gain Set = 10 dB (G_{10})	**NF_{BACK}**		5.5	5.8	dB
Output IP3 - Max Gain	▪ Set G_{MAX}, ▪ T_{AMB} = 25C ▪ Pout = +3 dBm per tone ▪ 800 KHz Tone Separation	**$IP3_{O1}$**	***42***	***48***		dBm

IDTF1241 SPECIFICATION (CONT.)

Parameter	Comment	Symbol	min	typ	max	units
Output IP3 - Mid Gain	▪ Set Gain = 10 dB (G_{10}) ▪ Pout = +3 dBm per tone ▪ 800 KHz Tone Separation	**$IP3_{O2}$**		45.1		dBm
2nd Harmonic	▪ Set G_{10} ▪ Pout = +3 dBm	**H2**		-82		dBc
Output IP2	▪ Set G_{10} ▪ 800 KHz Tone Separation ▪ Pout = +3 dBm per tone	**$IP2_H$**		77		dBm
1 dB Compression	Measured @ G_{20}	**$P1dB_O$**	***17***	***20.4***		dBm
Channel Isolation	OUT_B vs. OUT_A w/ IN_A input ▪ Measured @ G_{20} for both channels	**ISO_C**		68		dBc
Settling Time	▪ Any two Adjacent 1dB Steps ▪ +/-0.10 dB Pout settling	**T_{1dB}**		15		nsec

SPECIFICATION NOTES:

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test

2 – All other Items in min/max columns are Guaranteed by Design Centering

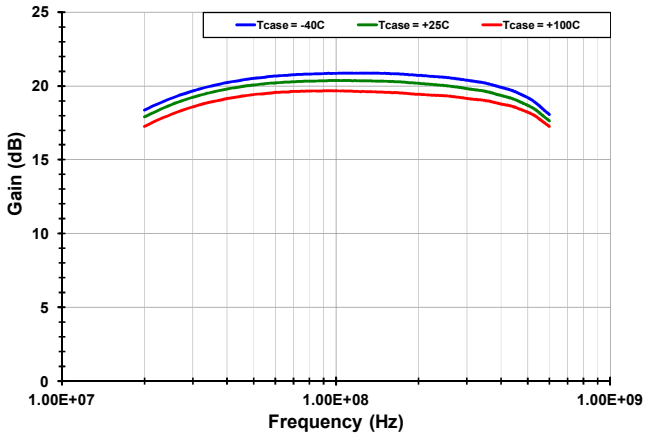
3 - STBY_A, and STBY_B both have internal pullup resistors such that they float to > V_{IH}

4 - Measured with 4:1 Transformers (see applications Circuit)

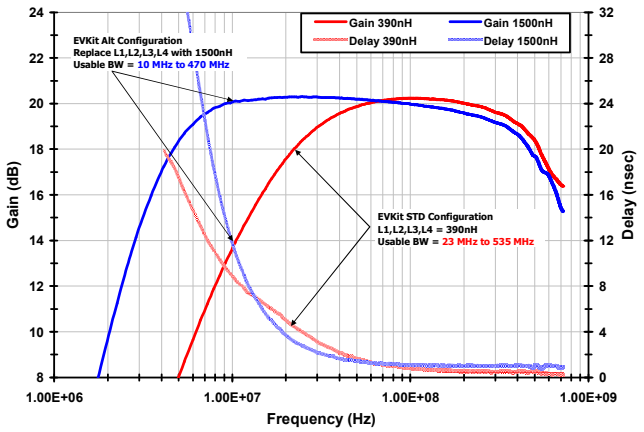
TYPICAL OPERATING CURVES (G_{MAX}, 5.00V, T_{CASE} = 25C, 200 MHz, TC4 de-embedded unless otherwise noted)

All temperatures are T_{CASE} unless noted as T_{AMB} or T_A = Ambient

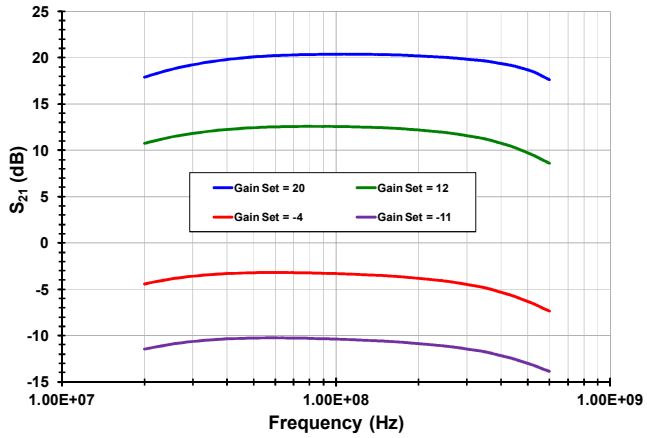
Gain vs. Frequency [Gain Set = 20 dB]



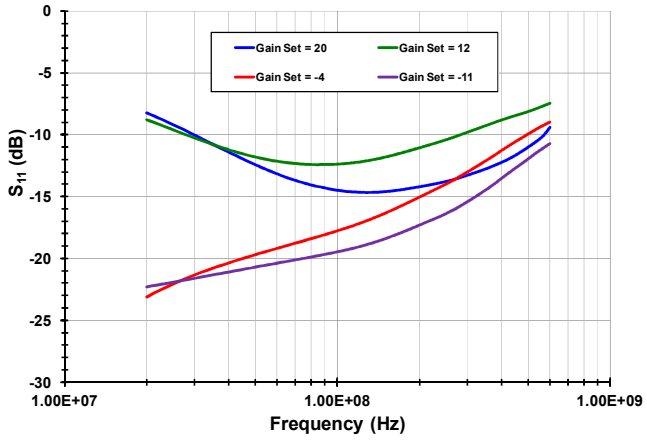
Extended Applications Range [T_{AMB} = 25C]



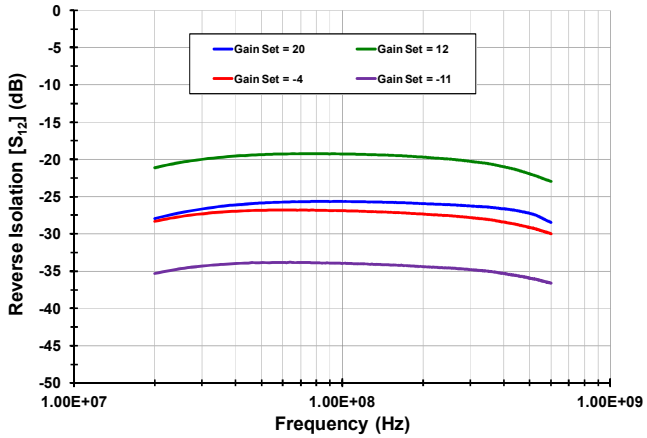
S_{21} vs. Frequency [T_{CASE} = 25C]



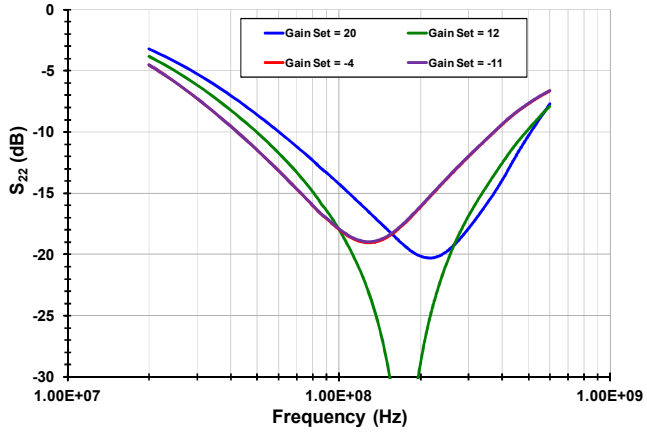
S_{11} vs. Frequency [T_{CASE} = 25C]



S_{12} vs. Frequency [T_{CASE} = 25C]

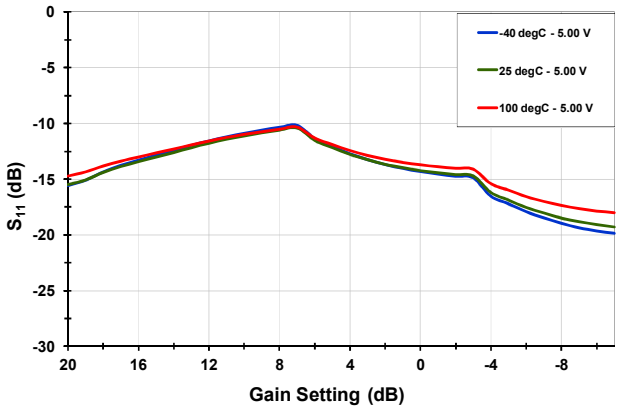


S_{22} vs. Frequency [T_{CASE} = 25C]

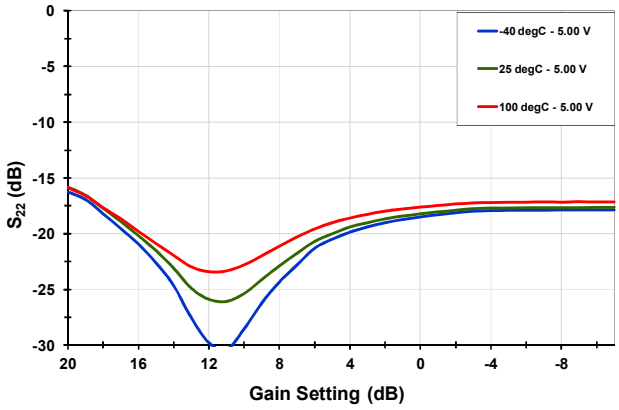


TOCs CONTINUED (-2-)

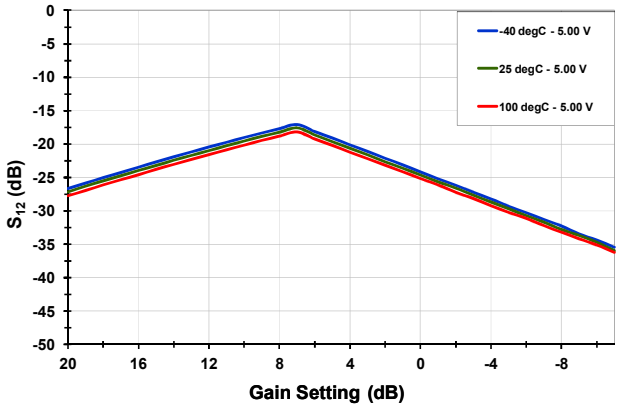
S_{11} vs. Gain Setting [200 MHz]



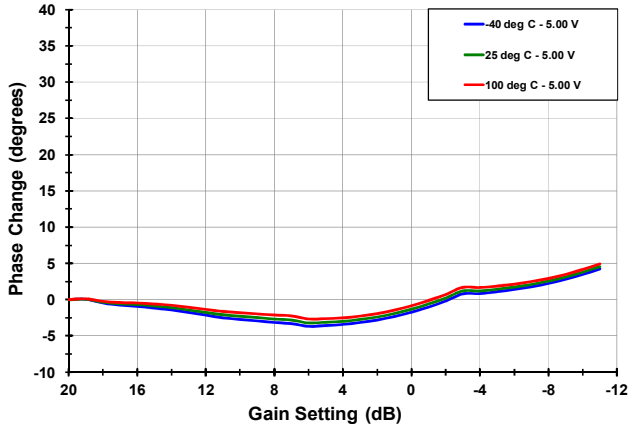
S_{22} vs. Gain Setting [200 MHz]



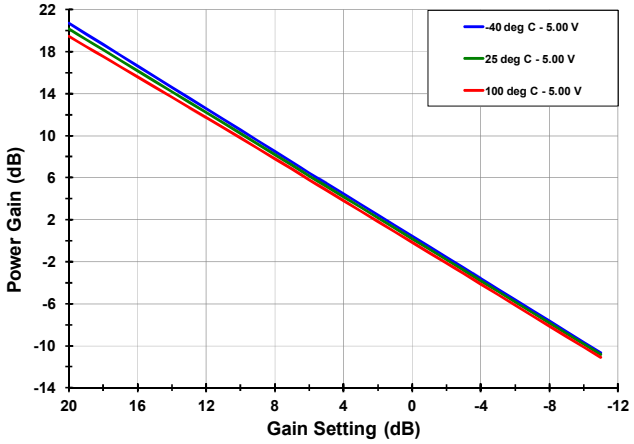
S_{12} vs. Gain Setting [200 MHz]



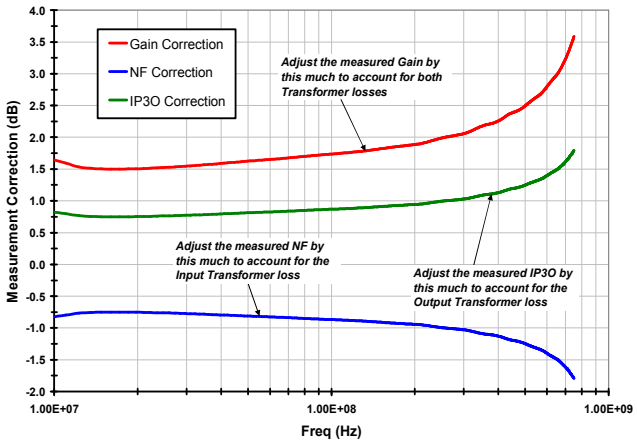
Phase Error vs. Gain Setting [200 MHz]



S_{21} vs. Gain Setting [200 MHz]

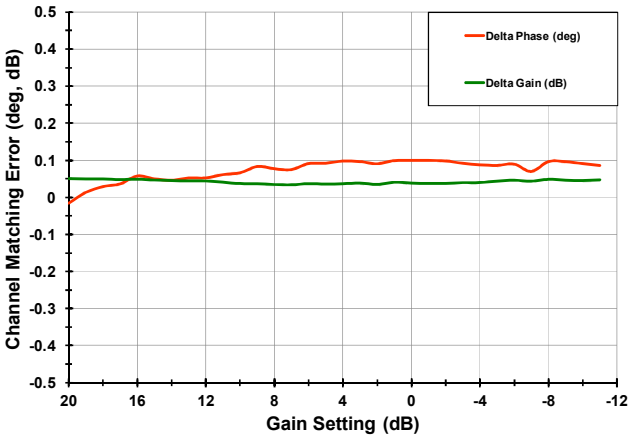


EVKit Measurement Corrections [TC4-1W, T_{AMB}]

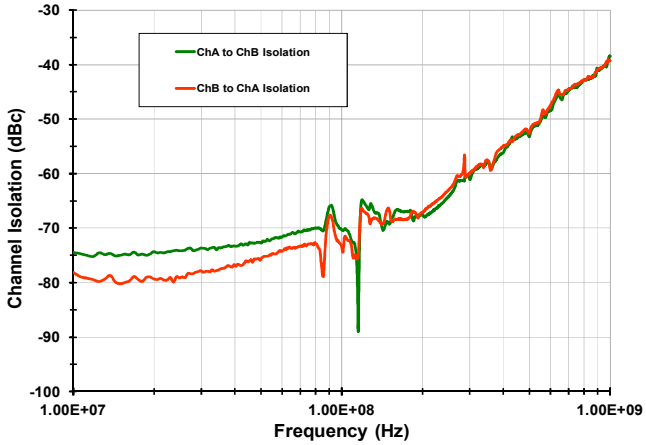


TOCs CONTINUED (-3-)

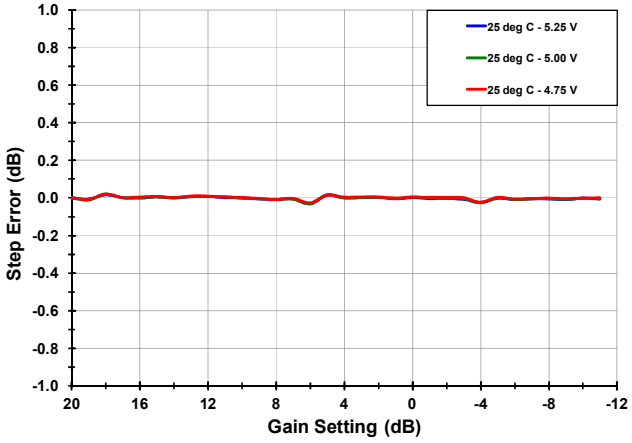
Channel Matching [200 MHz, T_{CASE} = 25C]



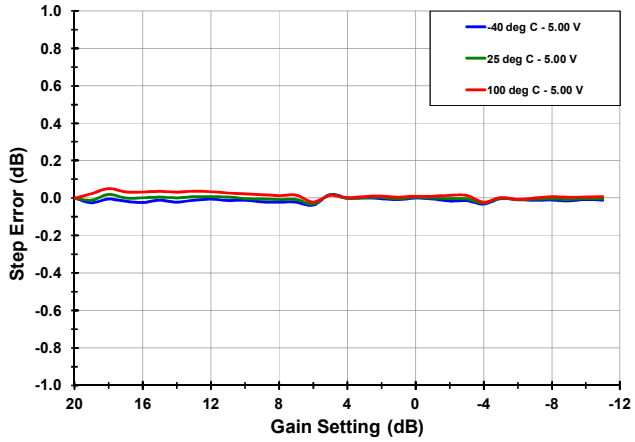
Channel Isolation vs. Frequency [T_{AMB} = 25C]



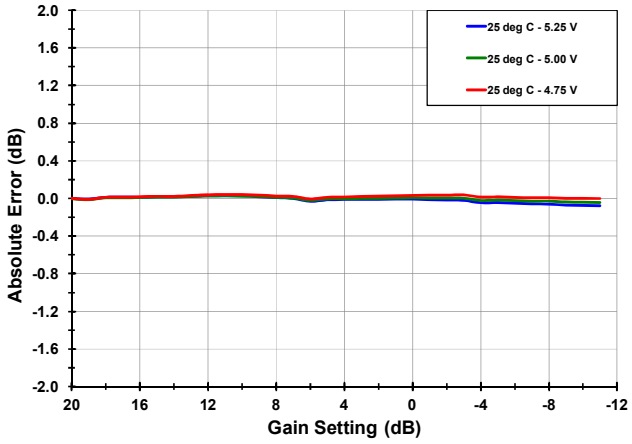
DNL vs. V_{CC} [200 MHz]



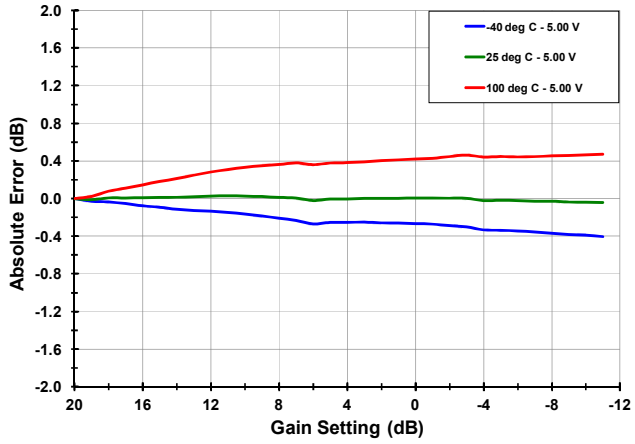
DNL vs. T_{CASE} [200 MHz]



INL vs. V_{CC} [200 MHz]

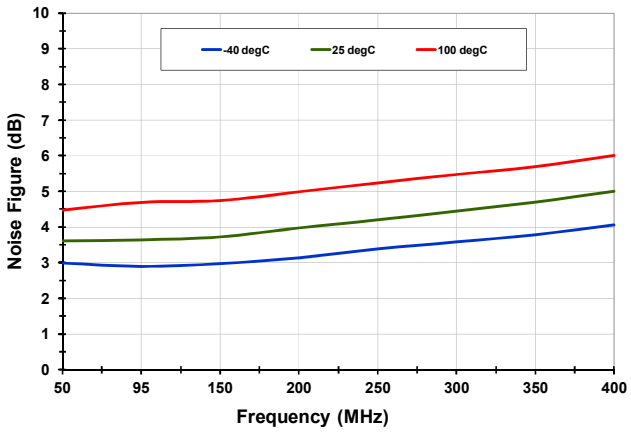


INL vs. T_{CASE} [200 MHz]

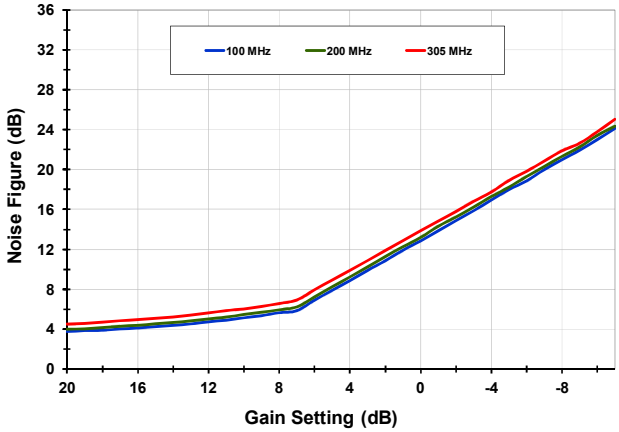


TOCs CONTINUED (-4-)

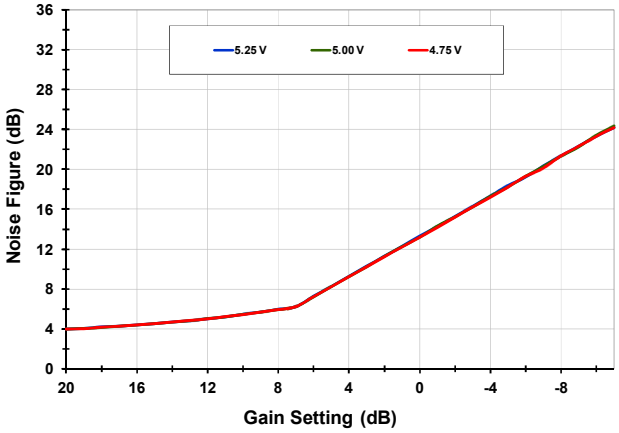
Noise Figure vs. Frequency [Gain Set = 20 dB]



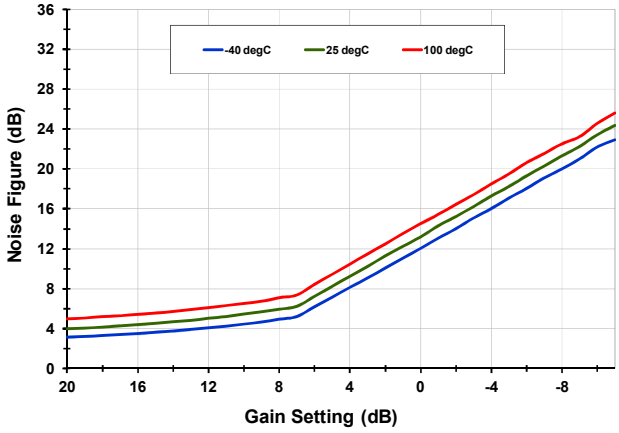
Noise Figure vs. Gain Setting [T_{CASE} = 25C]



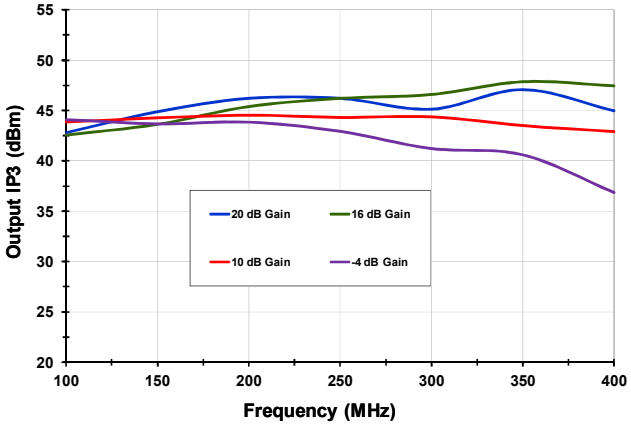
Noise Figure vs. V_{CC} [200 MHz]



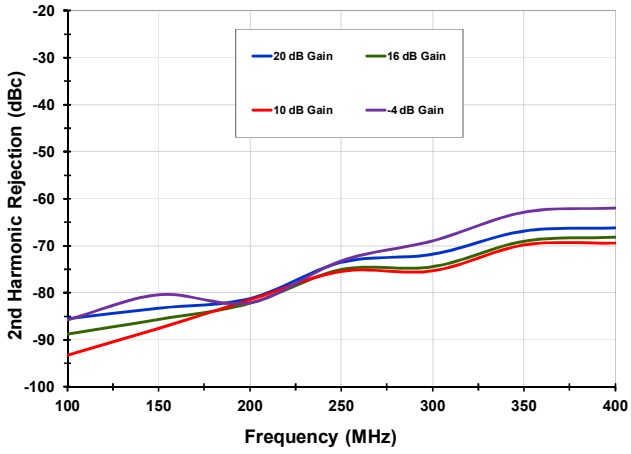
Noise Figure vs. T_{CASE} [200 MHz]



Output IP3 vs. Frequency [T_{CASE} = 25C]

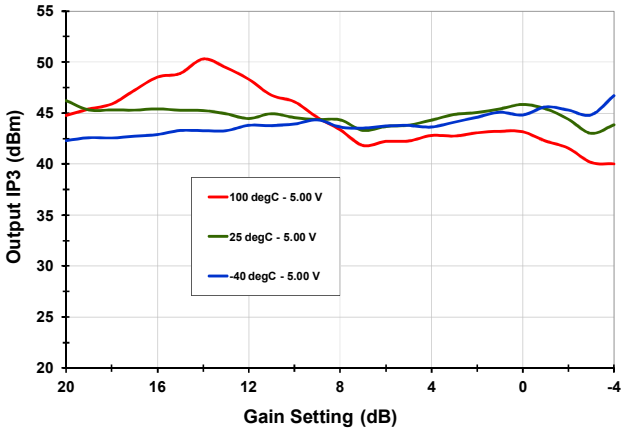


2nd Harmonic vs. Frequency [T_{CASE} = 25C]

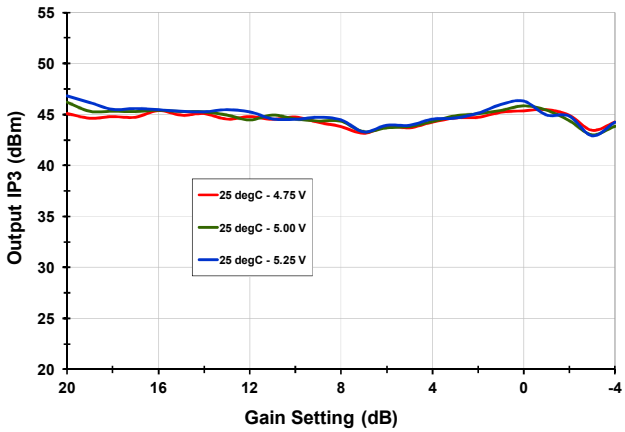


TOCs CONTINUED (-5-)

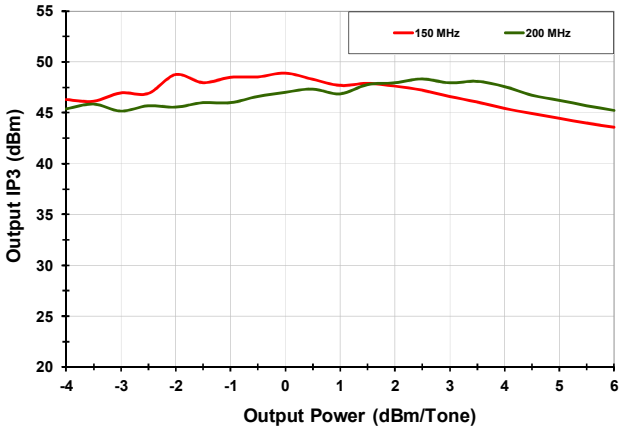
Output IP3 vs. T_{CASE} [200 MHz]



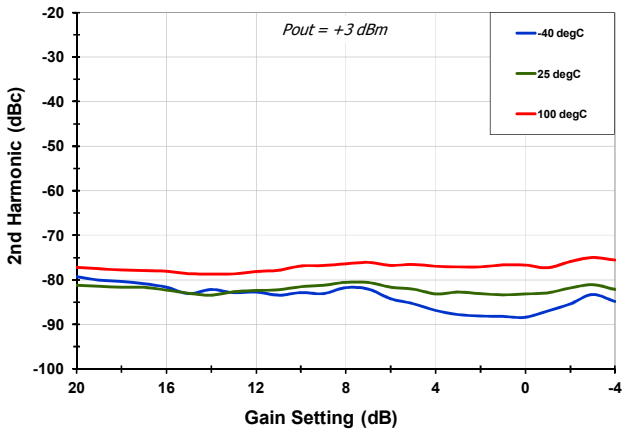
Output IP3 vs. V_{CC} [200 MHz]



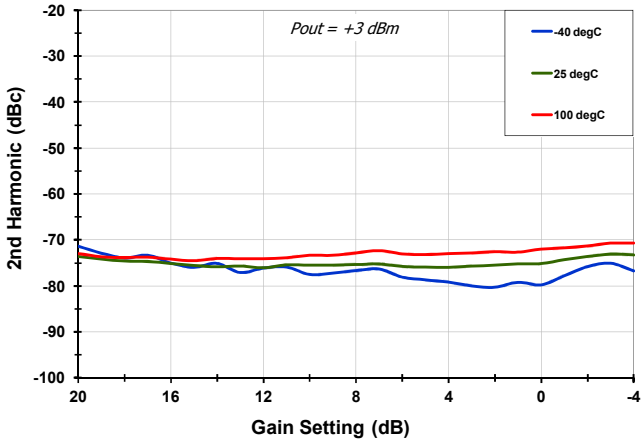
Output IP3 vs. Pout [T_{AMB} = 25C, Gain Set = 20 dB]



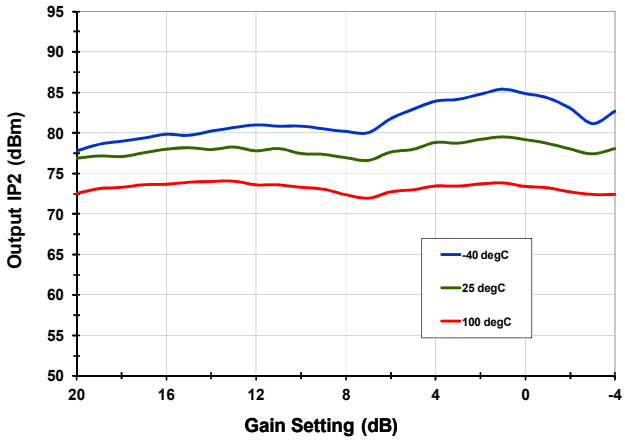
2nd Harmonic vs. T_{CASE} [200 MHz]



2nd Harmonic vs. T_{CASE} [250 MHz]

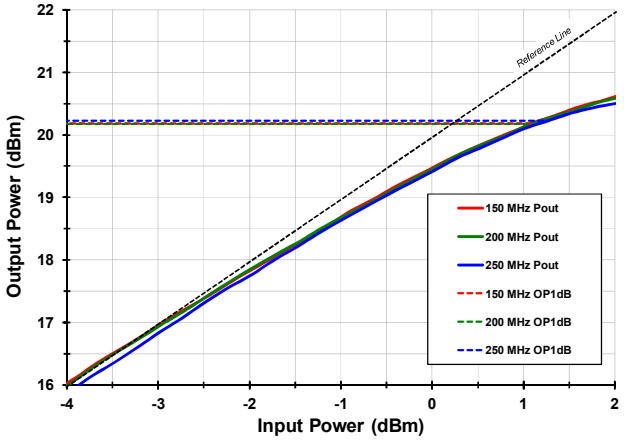


Output IP2 vs. T_{CASE} [200 MHz]

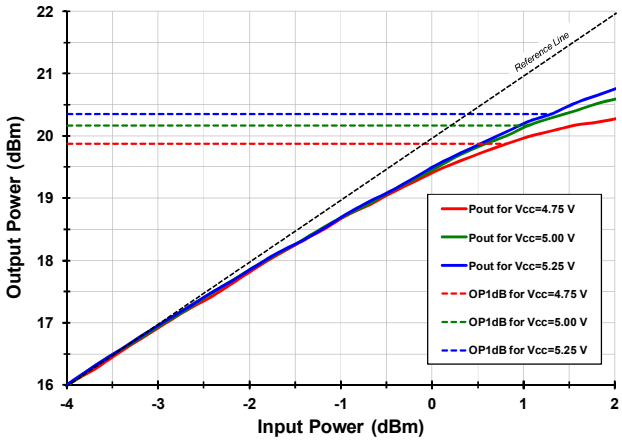


TOCs CONTINUED (-6-)

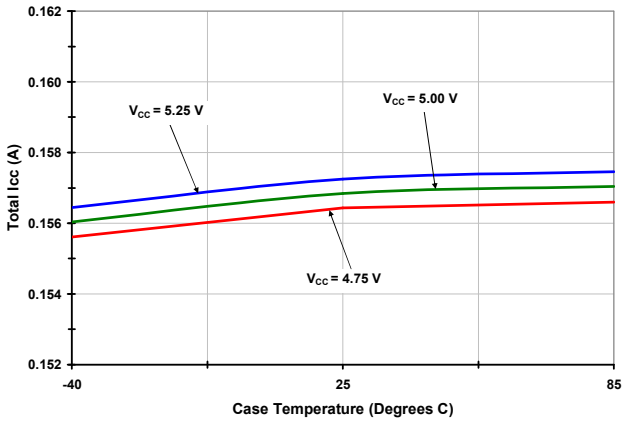
Gain Compression vs. Frequency [T_{AMB} = 25C]



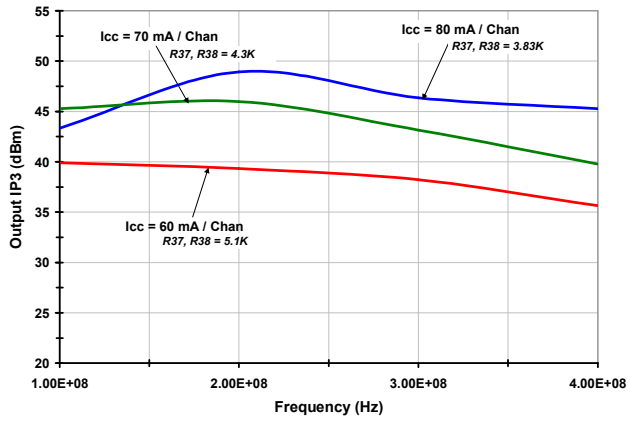
Gain Compression [200 MHz, T_{AMB} = 25C]



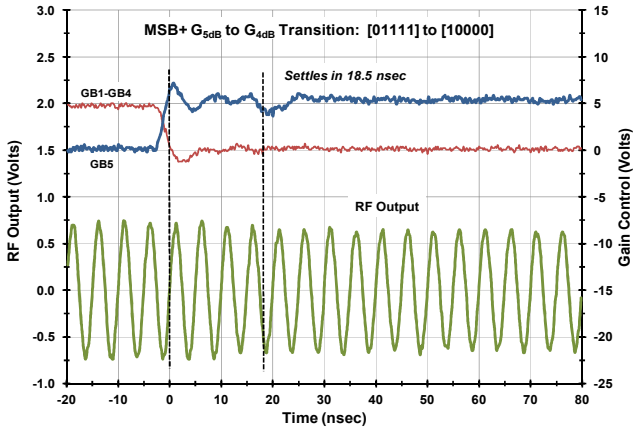
I_{CC} vs. T_{CASE}



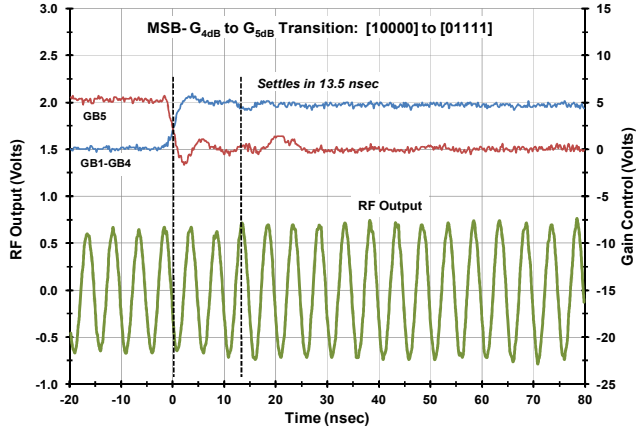
Output IP3 vs. I_{CC} [T_{AMB} = 25C]



Settling Time [1dB Step, 200 MHz, MSB+]



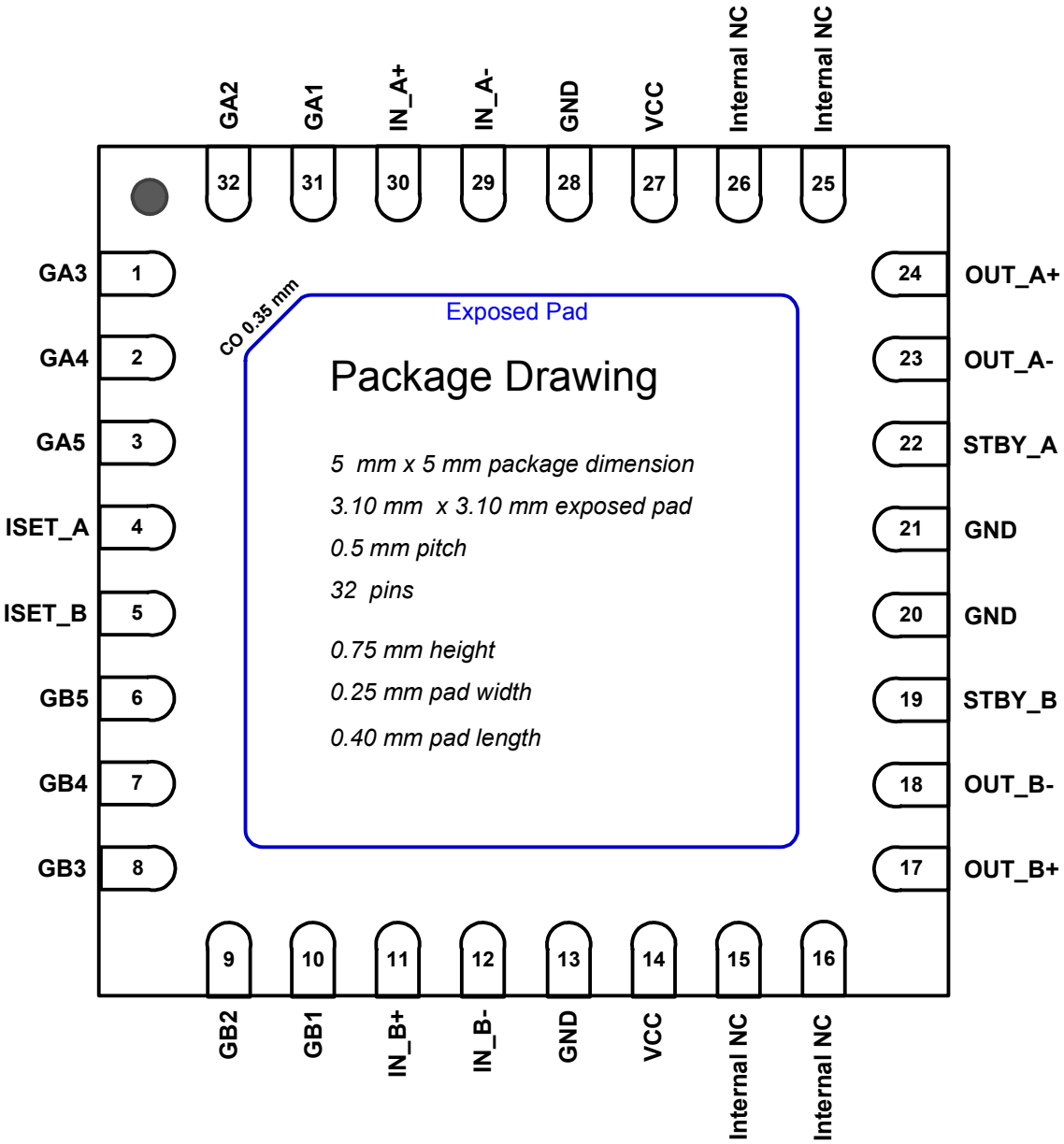
Settling Time [1dB Step, 200 MHz, MSB-]



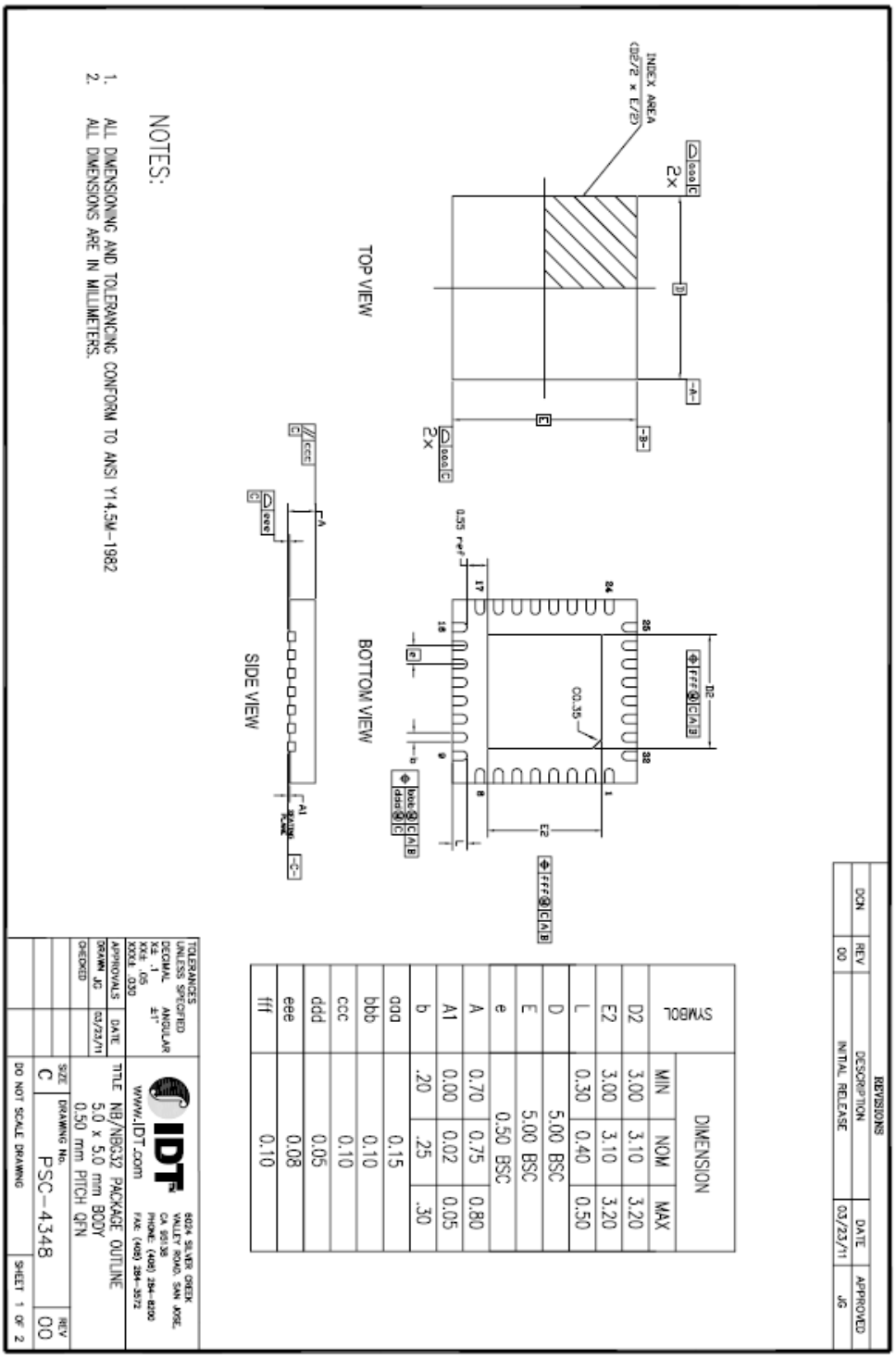
PIN DIAGRAM (F1241 – COMPATIBLE W/ADI AND BGA DEVICES)

Note: STBY_A, and STBY_B have internal Pullup resistors

TOP View
(looking through the top of the package)



PACKAGE DRAWING

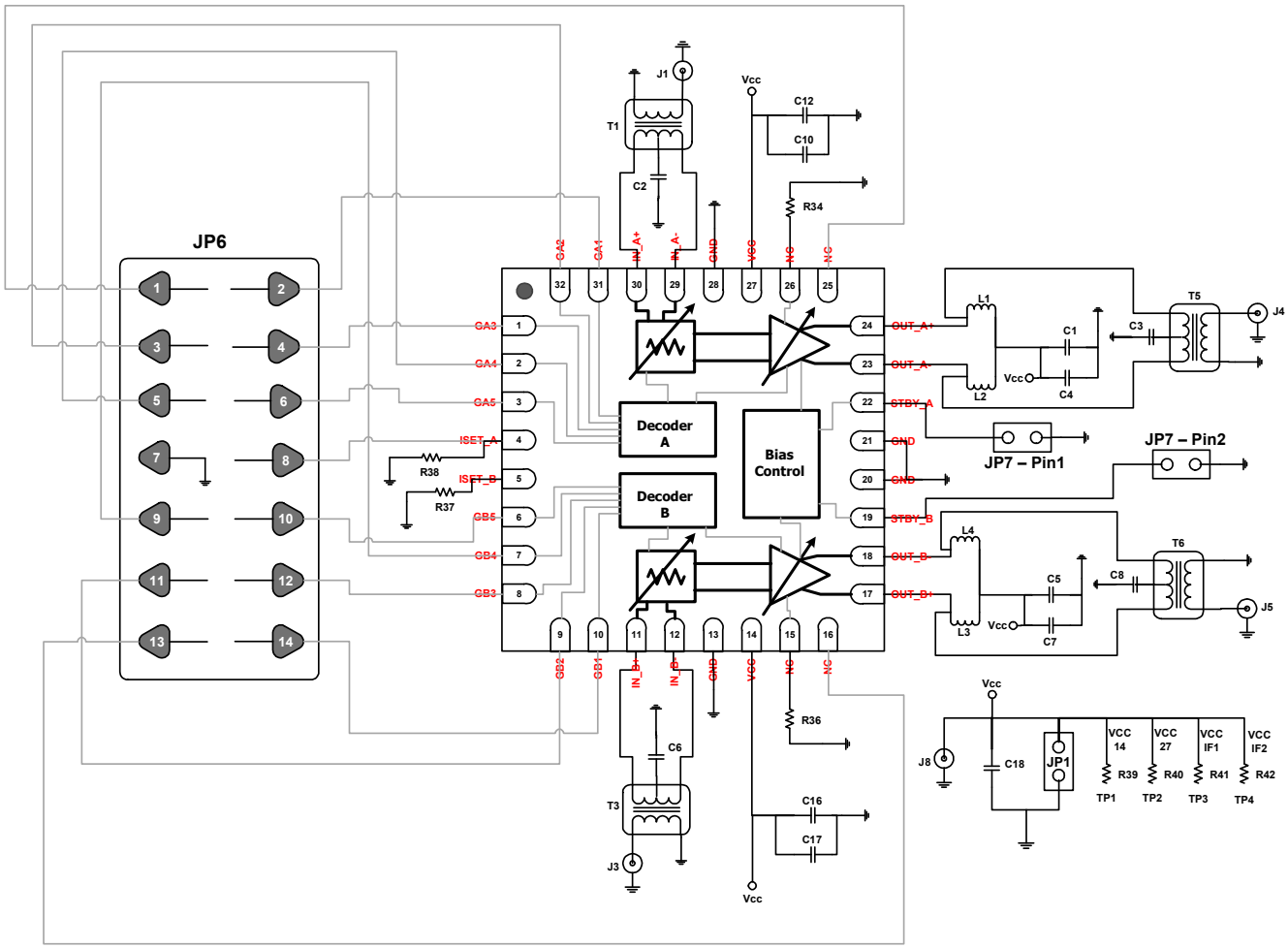


PIN DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	GA3	4 dB ATTN ctrl bit for Channel A
2	GA4	8 dB ATTN ctrl bit for Channel A
3	GA5	16 dB ATTN ctrl bit for Channel A
4	ISET_A	ChA Icc set: Use the recommended value from the BOM section
5	ISET_B	ChB Icc set: Use the recommended value from the BOM section
6	GB5	16 dB Attenuation ctrl bit for Channel B: 1 or high = 16 dB ATTN
7	GB4	8 dB Attenuation ctrl bit for Channel B: 1 or high = 8 dB ATTN
8	GB3	4 dB Attenuation ctrl bit for Channel B: 1 or high = 4 dB ATTN
9	GB2	2 dB Attenuation ctrl bit for Channel B: 1 or high = 2 dB ATTN
10	GB1	1 dB Attenuation ctrl bit for Channel B: 1 or high = 1 dB ATTN
11	IN_B+	Channel B Differential Input +. AC couple
12	IN_B-	Channel B Differential Input -. AC couple
13	GND	Connect this pin to Ground
14	VCC	Connect this pin to the 5V DC Power Bus
15	NC	Internally Unconnected
16	NC	Internally Unconnected
17	OUT_B+	Channel B Differential Output +. Pull up to Vcc through an inductor
18	OUT_B-	Channel B Differential Output-. Pull up to Vcc through an inductor
19	STYB_B	Pull low to Power Down ChB. Float or Pull high to enable ChB
20	GND	Connect this pin to Ground
21	GND	Connect this pin to Ground
22	STYB_A	Pull low to Power Down ChA. Float or Pull high to enable ChA
23	OUT_A-	Channel A Differential Output -. Pull up to Vcc through an inductor
24	OUT_A+	Channel A Differential Output +. Pull up to Vcc through an inductor
25	NC	Internally Unconnected
26	NC	Internally Unconnected
27	VCC	Connect this pin to the 5V DC Power Bus
28	GND	Connect this pin to Ground
29	IN_A-	Channel A Differential Input -. AC couple
30	IN_A+	Channel B Differential Input +. AC couple
31	GA1	1 dB Attenuation ctrl bit for Channel A
32	GA2	2 dB ATTN ctrl bit for Channel A
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal relief

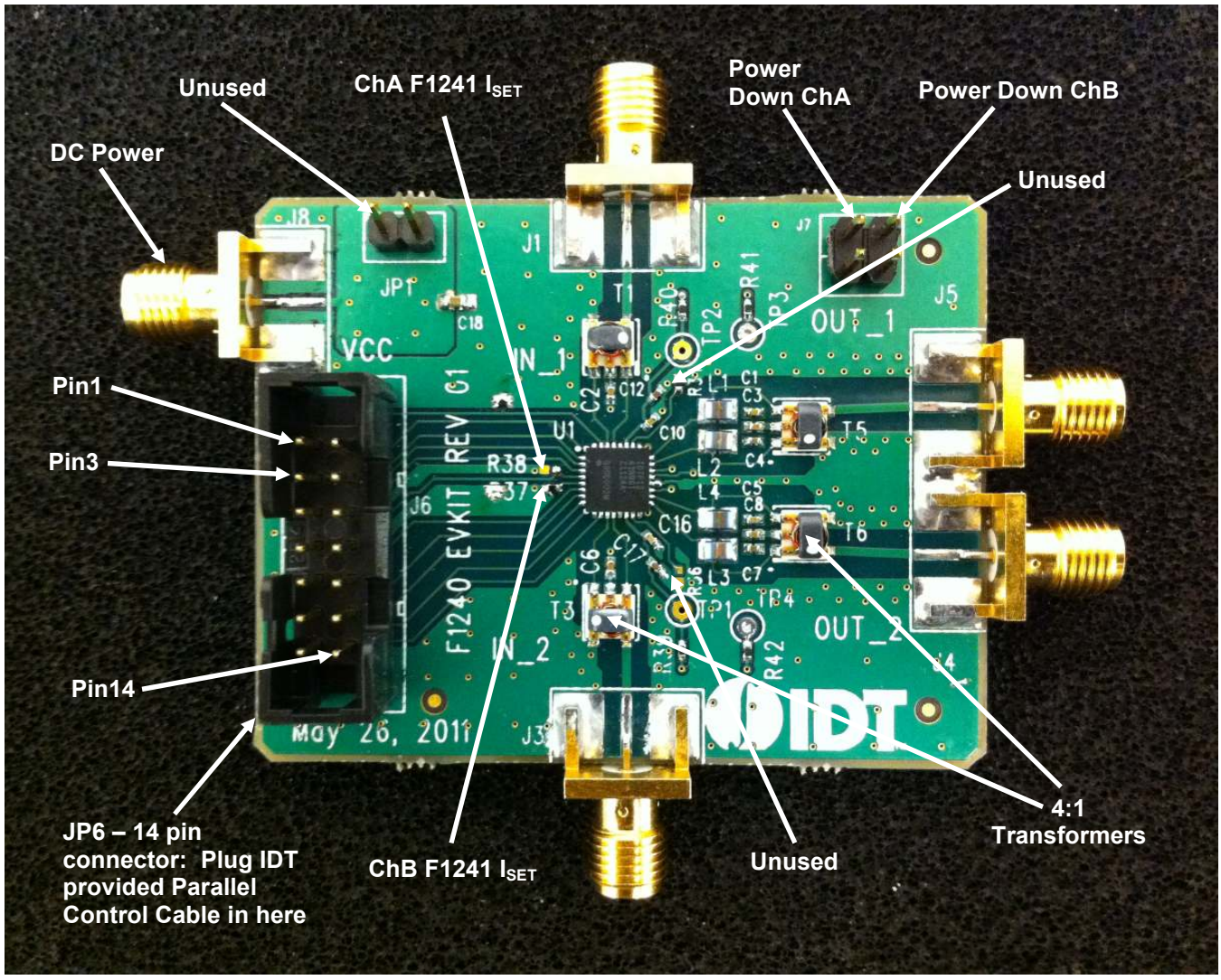
EVKIT SCHEMATIC

The diagram below describes the recommended applications / EVkit circuit:



EVKIT OPERATION (Email: RFsupport@IDT.com to request an EVkit and Control Cable)

The picture and graphic below describe how to operate the EVkit



EVKIT BOM (F1241)

REF DES	VALUE	CASE SIZE	MFG		REF DES	VALUE	CASE SIZE	MFG
R34	DNP	0402			C7	0.1 uF	0402	
R36	DNP	0402			C8	0.1 uF	0402	
R37	3.83K +/-1%	0402			C10	1,000 pF	0402	
R38	3.83K +/-1%	0402			C12	0.1 uF	0402	
R39	0 ohm	0402			C16	1,000 pF	0402	
R40	0 ohm	0402			C17	0.1 uF	0402	
R41	0 ohm	0402			C18	10 uF	0603	
R42	0 ohm	0402			T1	4:1	TC4-1WG2+	MiniCircuits
L1	390 nH	0805	Coilcraft		T3	4:1	TC4-1WG2+	MiniCircuits
L2	390 nH	0805	Coilcraft		T5	4:1	TC4-1WG2+	MiniCircuits
L3	390 nH	0805	Coilcraft		T6	4:1	TC4-1WG2+	MiniCircuits
L4	390 nH	0805	Coilcraft		J1	SMA		
C1	1,000 pF	0402			J3	SMA		
C2	0.1 uF	0402			J4	SMA		
C3	0.1 uF	0402			J5	SMA		
C4	0.1 uF	0402			J8	SMA		
C5	1,000 pF	0402			JP1	DNP		
C6	0.1 uF	0402			J6	14 pin- CTRL		
					J7	4 pin - STBY		

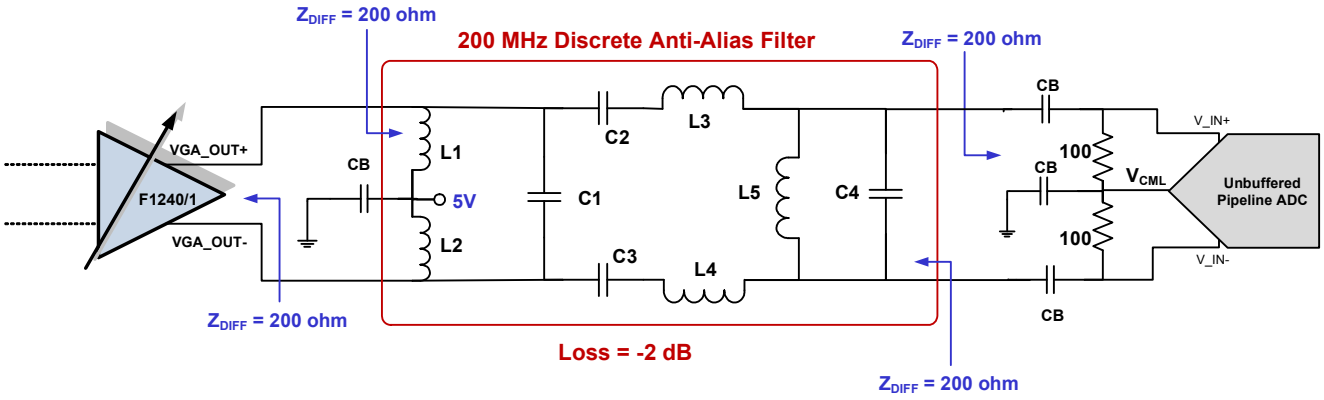
APPLICATIONS INFORMATION

The F1241 has been optimized for use in high performance IF sub-sampling applications. It has unique features that make it ideal for these very demanding applications.

Noise Contour

The remarkable FlatNoise™ feature of the device (see first four graphs on page 10) has great benefits when implemented in wideband multi-carrier systems. For the first 13 dB of attenuation range, the device has only 2.3 dB degradation in noise figure. This is in stark contrast to standard VGAs that have a linear dB-for-dB degradation in Noise Figure with increasing attenuation.

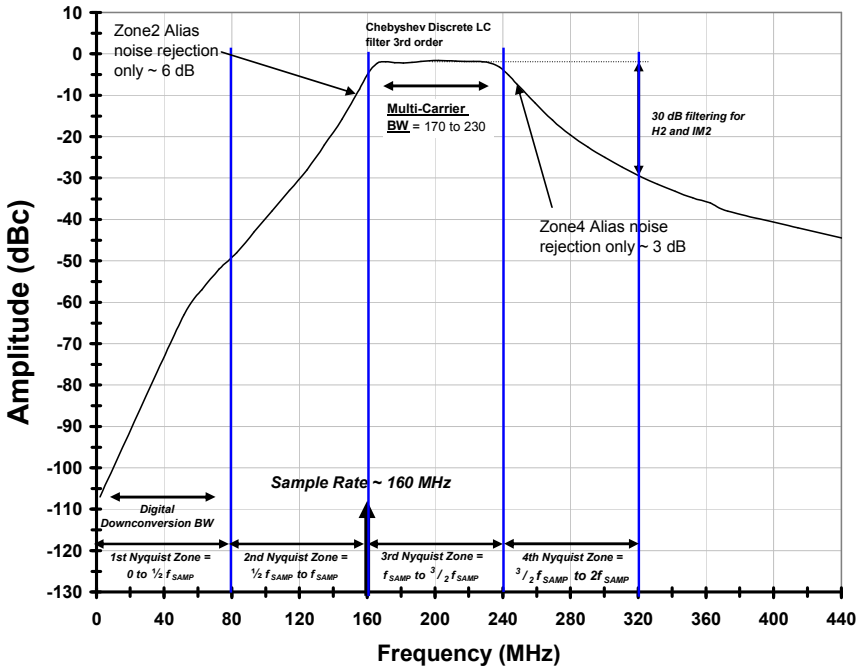
Refer to the figure below. It depicts the F1241 driving a matched Anti-Alias Filter which is followed by an ADC with a differential resistive 200 ohm termination. Note that at each point in the system the matching is preserved.



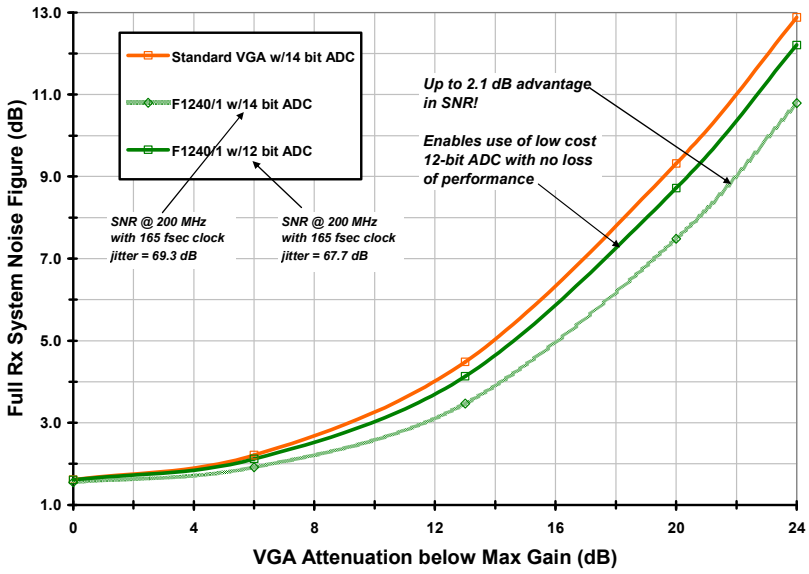
A discrete realization of a 3rd order Anti-Alias filter is shown on the next page. Sampling occurs in Nyquist Zone3 for a 60 MHz multi-carrier signal. Noise just 20 MHz above & below the signal bandedges will alias from either Zone4 or Zone2 and show up as added noise in the desired band at the digital output of the ADC.

APPLICATIONS INFORMATION (CONT.)

Noise Contour (cont.)



The result is that the F1241 with its unique noise contour will improve SNR significantly in this multi-carrier instance . Note in the graph below: SNR improves over 2 dB at high attenuation settings which allows for the use of a lower cost / lower resolution ADC in the Rx path. Alternately, F1241 FlatNoise™ coupled with its excellent H2, IM2, and H3 performance allows simplification or even elimination of the Anti-Alias Filter.



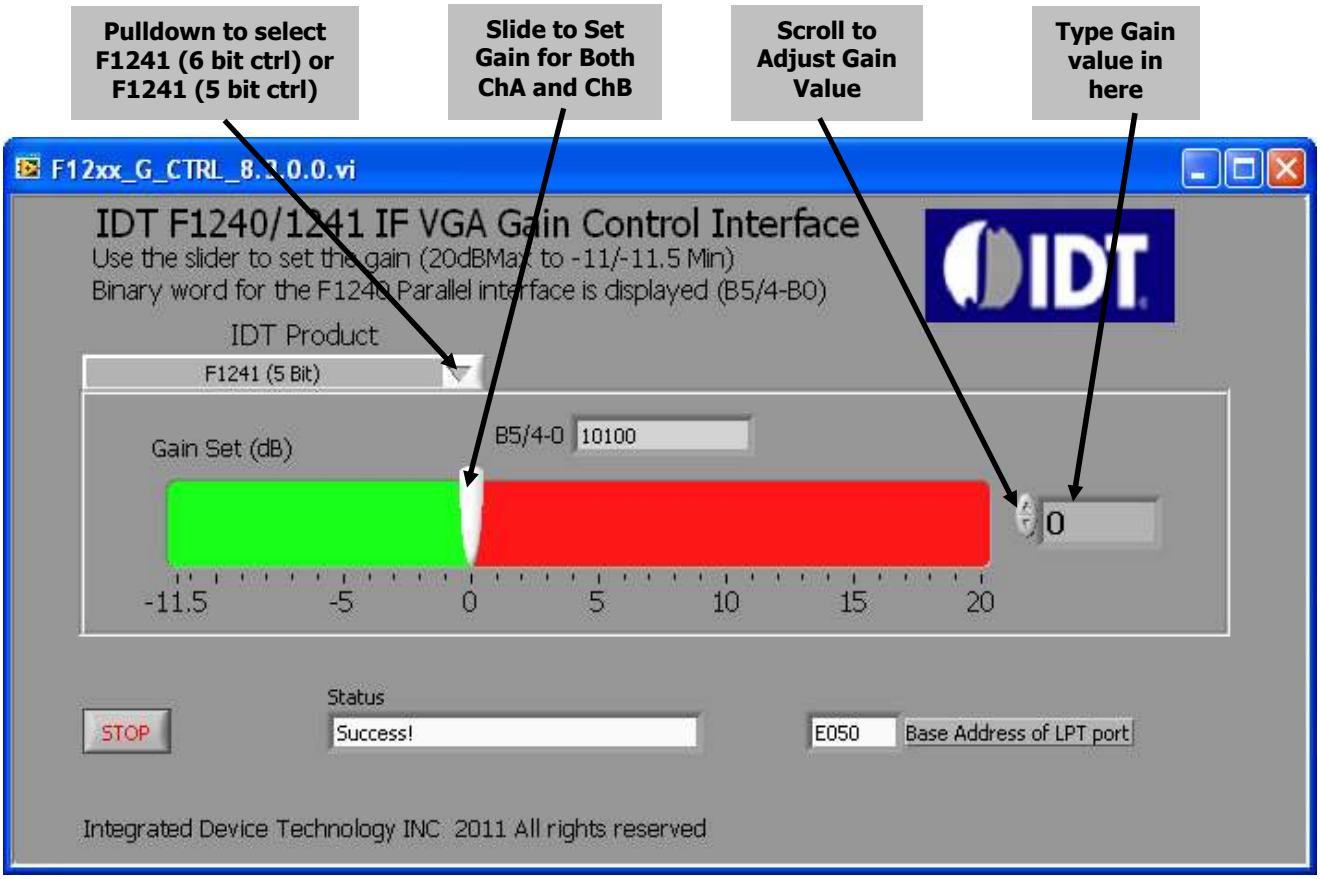
APPLICATIONS INFORMATION (CONT.)

Other Key Features:

Current Setting Resistors – The IDTF1241 already offers the best IM3 distortion performance over the widest Power range when driving a matched load w/ 160 mA Total I_{CC}. The user has the option to reduce I_{CC} even further at the expense of Output IP3. See the graph at Middle Right on Page 10 for details. Note that ChA and ChB I_{CC} can be independently set.

Settling Time – The IDTF1241 has been designed as Glitch-Free™ when changing gain between **ANY** adjacent steps. Note the two graphs at the bottom of Page 10. Even for 1 dB steps that involve **MSB transitions** the settling time is still <15 nsec.

Gain Controller Software



Connect IDT Cable to 14 pin connector on EVkit

Connect IDT Cable to 'Parallel Port' of Desktop PC

Download Controller Software:

- Point your browser to: ftp://ftp3.idt.com
- User Name: prodemo
- Password: Fa9HsG2I
- File Name: F12xx_G_CTRL_8.4.2.0.zip
- Run setup.exe right from the zip file…

Contact your IDT Sales Professional or Email: RFsupport@IDT.com to request applications support

APPLICATIONS INFORMATION (CONT.)

Operation into a 100 ohm load

The F1241 can be dropped directly into a 100 ohm termination environment without any topology changes, so no board redesign is necessary. The example schematic below is for a 153 MHz IF center frequency. Simply replace the pullup inductors already on the board with 91 nH and replace the series AC coupling capacitors already on the board with 18 pF. The F1241 in this case will then drive a 100 ohm filter with ~16 dB return loss. See schematic and measured results when matched to 100 ohms below: