High Voltage Three Phase Gate Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: September 1, 2016

Recommended Substitutions: no direct replacement

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

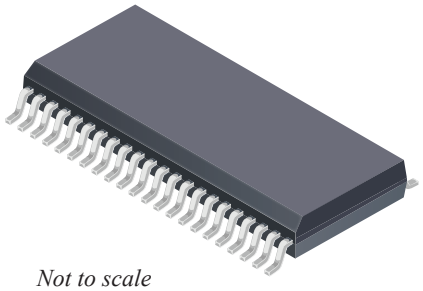
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

High Voltage Three Phase Gate Driver

Features and Benefits

- High voltage 3-phase gate drive
- Floating high-side gate drive to 550 VDC supply
- Tolerant to high voltage slew rates
- Cross-conduction protection with fixed dead time
- 15 V gate drive supply voltage
- TTL compatible logic inputs
- Undervoltage detection
- Overcurrent detection with integrated fault blanking
- Overtemperature shutdown
- Matched propagation delays
- Detailed fault reporting

Package: 44-pin QSOP (suffix LQ)



Not to scale

Description

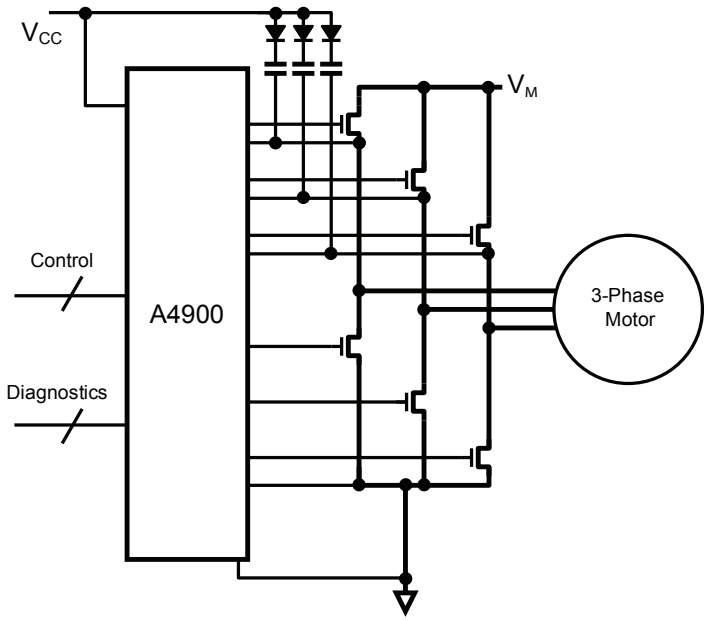
The A4900 is a high-voltage, high-speed, power IGBT or MOSFET driver providing three independent half-bridge channels for three-phase applications.

A bootstrap capacitor is used to provide the above battery supply voltage required for N-channel MOSFETs or IGBTs used as high current switches. Direct control over all six gate drives in the 3-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation. The power switches are protected from cross-conduction by integrated crossover control and fixed dead time.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults. They can be configured to protect the power switches under most short circuit conditions. Detailed diagnostics are available as a serial data word output.

The A4900 is provided in a 44-pin QSOP package (suffix LQ) that is lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application Diagram



Selection Guide

Part Number	Operating Ambient Temperature Range T_A, (°C)	Package	Packing
A4900KLQTR-T	–40 to 125	44-pin QSOP	1000 pieces per 13-in. reel

Absolute Maximum Ratings with respect to GND

Characteristic	Symbol	Notes	Rating	Unit
Drive Supply Voltage	V_{CC}		–0.3 to 20	V
Logic Input and Output Voltage		Pins AHI, ALO, BHI, BLO, CHI, CLO, COASTn, RESETn, ESF, FF1, and FF2	–0.3 to 6.5	V
Other Pins Input and Output Voltage		Pins BCA, BCB, BCC	–0.3 to Sx+20	V
		Pins GHA, GHB, GHC	Sx – 0.3 to BCx + 0.3	V
		Pins SA, SB, SC	$-V_{CC}$ to 600	V
		Pins GLA, GLB, GLC	–0.3 to V_{CC} + 0.3	V
Clamp Current	I_{DCL}	Pins DHA, DHB, DHC, DLA, DLB, DLC	1	mA
Maximum Voltage Slew Rate on Sx	dv_{Sx}/dt		50	V/ns
Ambient Operating Temperature Range	T_A	Temperature Range K	–40 to 125	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		150	°C
Transient Junction Temperature	T_{tJ}	Overtemperature event not exceeding 10 s, lifetime duration not exceeding 10 h; characterized by design	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	35	ºC/W

*Additional thermal information available on the Allegro website.

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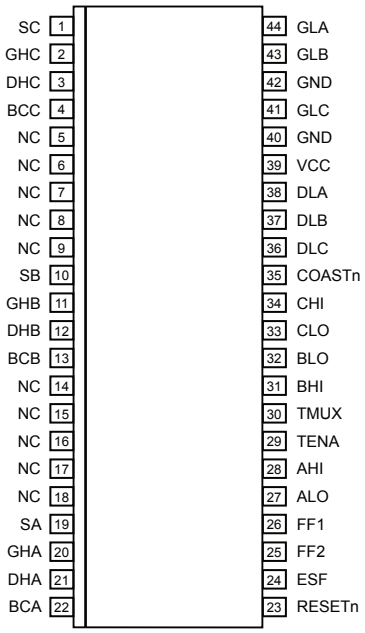
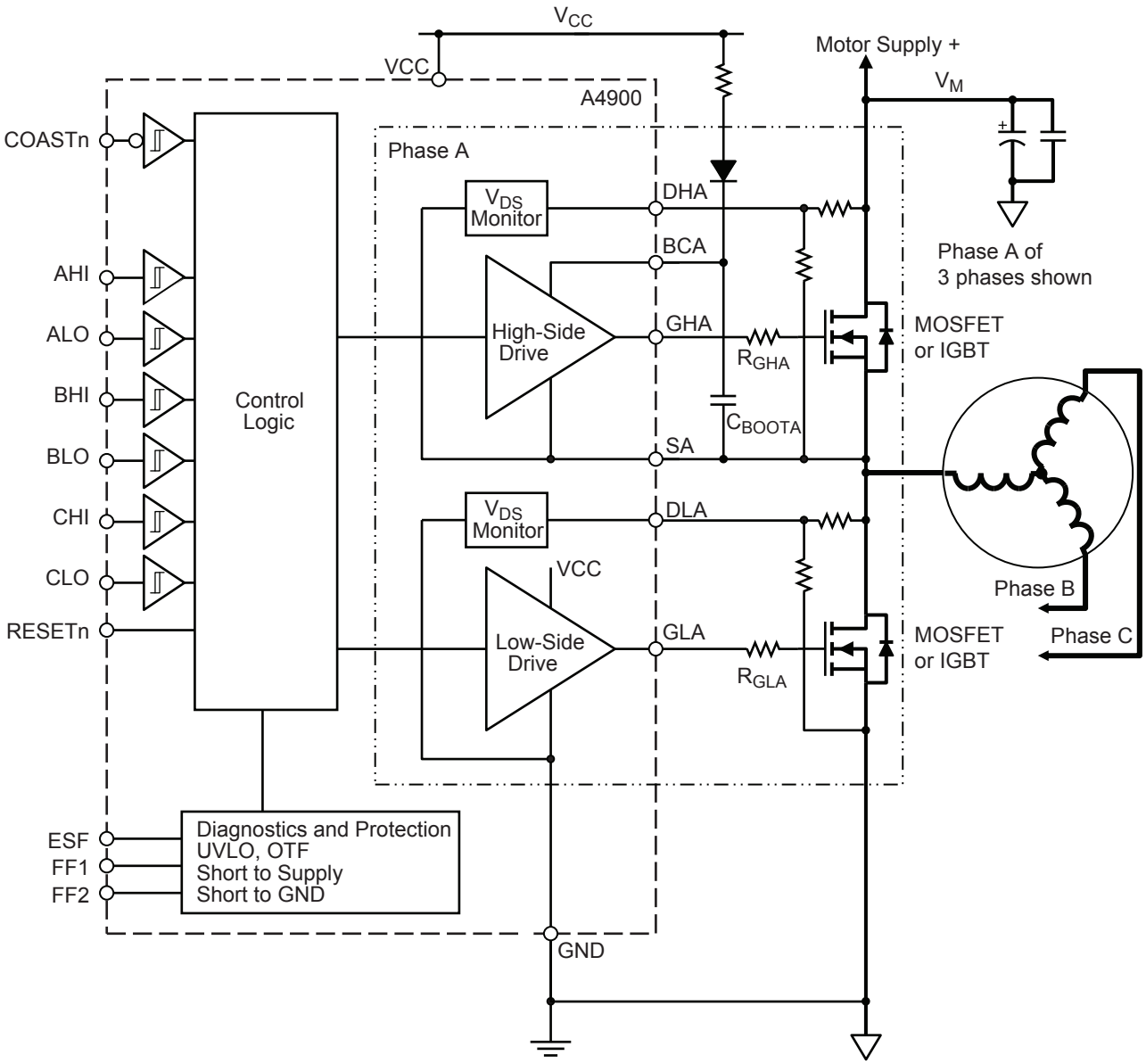
Pin-out Diagram



Terminal List Table

Name	Number	Function
AHI	28	Phase A high-side control logic input
ALO	27	Phase A low-side control logic input
BCA	22	Phase A high-side bootstrap supply capacitor (HVA)
BCB	13	Phase B high-side bootstrap supply capacitor (HVB)
BCC	4	Phase C high-side bootstrap supply capacitor (HVC)
BHI	31	Phase B high-side control logic input
BLO	32	Phase B low-side control logic input
CHI	34	Phase C high-side control logic input
CLO	33	Phase C low-side control logic input
COASTn	35	Motor coast logic input, active low
DHA	21	Phase A high-side drain voltage monitor input (HVA)
DHB	12	Phase B high-side drain voltage monitor input (HVB)
DHC	3	Phase C high-side drain voltage monitor input (HVC)
DLA	38	Phase A low-side drain voltage monitor input
DLB	37	Phase B low-side drain voltage monitor input
DLC	36	Phase C low-side drain voltage monitor input
ESF	24	Fail mode action control logic input
FF1	26	Fault flag 1 open drain output
FF2	25	Fault flag 2 open drain output
GHA	20	Phase A high-side FET gate drive (HVA)
GHB	11	Phase B high-side FET gate drive (HVB)
GHC	2	Phase C high-side FET gate drive (HVC)
GLA	44	Phase A low-side FET gate drive
GLB	43	Phase B low-side FET gate drive
GLC	41	Phase C low-side FET gate drive
GND	40, 42	Ground
NC	5, 6, 7, 8, 9, 14, 15, 16, 17, 18	Do not connect
RESETn	23	Reset and shutdown logic input, active low
SA	19	Phase A high-side FET source and motor phase (HVA)
SB	10	Phase B high-side FET source and motor phase (HVB)
SC	1	Phase C high-side FET source and motor phase (HVC)
TEST	29, 30	Connect to GND
VCC	39	Gate drive supply

Functional Block Diagram



ELECTRICAL CHARACTERISTICS Valid at T_J = –40°C to 150°C, V_{CC} = 15 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply						
VCC Supply Voltage	V_{CC}		13.5	15	16.5	V
VCC Quiescent Current	I_{VCCQ}	RESETn = high, outputs = low	–	8	10	mA
	I_{VCCS}	RESETn = low, sleep mode	–	–	80	µA
High-Side Driver Current	I_{BCxS}	Each phase	–	–	200	µA
Gate Output Drive						
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –100 mA	–	–	70	Ω
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 100 mA	–	–	35	Ω
Output High Short Circuit Pulsed Current	I_{OH}	V_O = 0 V, short pulse width (<10 µs)	–	210	–	mA
Output Low Short Circuit Pulsed Current	I_{OL}	V_O = 15 V short pulse width (<10 µs)	–	420	–	mA
GHx Output High Voltage	V_{GHH}		V_{BCx} – 0.2	–	–	V
GHx Output Low Voltage	V_{GHL}		–	–	V_{Sx} + 0.1	V
GLx Output High Voltage	V_{GLH}		V_{CC}–0.2	–	–	V
GLx Output Low Voltage	V_{GLL}		–	–	0.1	V
Turn-On Rise Time	t_r	C_{LOAD} = 1 nF, 20% to 80%	–	90	150	ns
Turn-Off Fall Time	t_f	C_{LOAD} = 1 nF, 80% to 20%	–	40	85	ns
Turn-Off Propagation Delay	$t_{P(off)}$	Phase input change to unloaded gate output change (see figure 1)	250	300	500	ns
		COASTn low to unloaded gate output change	370	420	570	ns
		RESETn low to unloaded gate output change	250	300	500	ns
Turn-On Propagation Delay	$t_{P(on)}$	Phase input change to unloaded gate output change (see figure 1)	250	300	500	ns
		COASTn high to unloaded gate output change	0.8	1	1.3	µs
Phase-to-Phase Propagation Delay Matching	Δt_{PP}	Same phase change	–	50	–	ns
On-to-Off Propagation Delay Matching	Δt_{OO}	Single phase	–	50	–	ns
High-Side Passive Pull-Down	R_{PDH}		–	800	–	kΩ
Low-Side Passive Pull-Down	R_{PDL}		–	800	–	kΩ
Dead Time[2]	t_{DEAD}	Delay from turn-off to turn-on, single phase	130	200	330	ns
Logic Inputs and Outputs						
FFx Fault Output (Open Drain)	V_{OL}	I_{OL} = 1 mA, fault not present	–	–	0.4	V
Fault Output Leakage Current*	I_{OH}	V_O = 5 V, fault present	–1	–	1	µA
Input Low Voltage	V_{IL}		–	–	0.7	V
Input High Voltage	V_{IH}		2.2	–	–	V
Input Hysteresis	V_{Ihys}		150	300	–	mV

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued) Valid at T_J = –40°C to 150°C, V_{CC} = 15 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Logic Inputs and Outputs (continued)						
Input Pull-Down Resistor	R_{PD}	All digital inputs	–	50	–	kΩ
RESETn Shutdown Time	t_{RSD}		10	–	–	µs
RESETn Start-up Time	t_{RSU}		–	15	20	µs
Reset Hold-Off Delay Time	t_{RHD}		–	5	–	µs
RESETn Pulse Time	t_{RES}		0.3	–	3.5	µs
RESETn Pulse Filter Time	t_{RF}		–	–	200	ns
Protection						
VCC Undervoltage Threshold	$V_{CCUVoff}$	V_{CC} falling	9	10	11	V
	V_{CCUVon}	V_{CC} rising	10	11	12	V
VCC Undervoltage Hysteresis	$V_{CCUVhys}$		–	1	–	V
Bootstrap Undervoltage Threshold	$V_{BCUVoff}$	BCx with respect to Sx, V_{BCx} falling	9	10	11	V
	V_{BCUVon}	BCx with respect to Sx, V_{BCx} rising	10	11	12	V
Bootstrap Undervoltage Hysteresis	$V_{BCUVHys}$		–	1	–	V
V_{DS} Threshold	V_{DSTH}		1.8	2.0	2.2	V
Drain Monitor Input Current	I_{DMH}	V_{DM} = 2.2 V (either $V_{DM} = V_{DHx} – V_{Sx}$, or $V_{DM} = V_{DLx}$)	–	–	100	nA
Drain Monitor Clamp Voltage	V_{DMC}		–	5	–	V
Drain Monitor Blank Time	t_{BL}		2	3	4.5	µs
Overtemperature Flag	T_{JF}	Temperature increasing	155	170	–	ºC
Overtemperature Hysteresis	T_{JHyst}	Recovery = $T_{JF} – T_{JHyst}$	–	15	–	ºC

*For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

Timing Diagrams

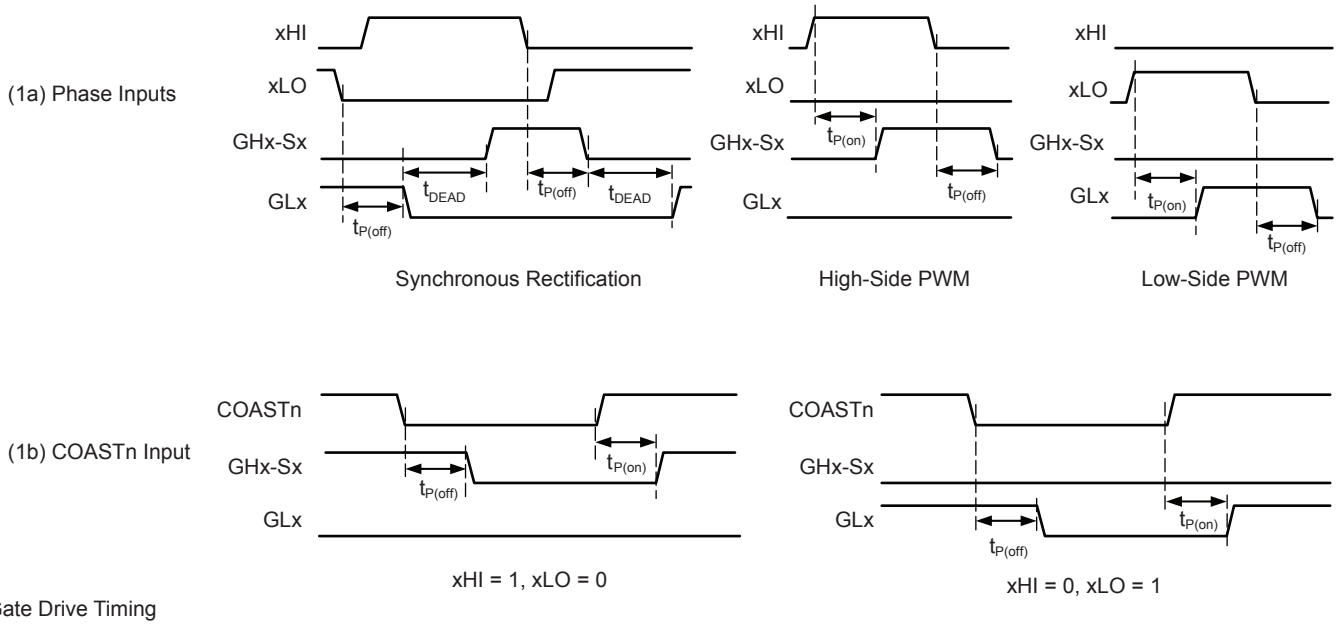


Figure 1. Gate Drive Timing

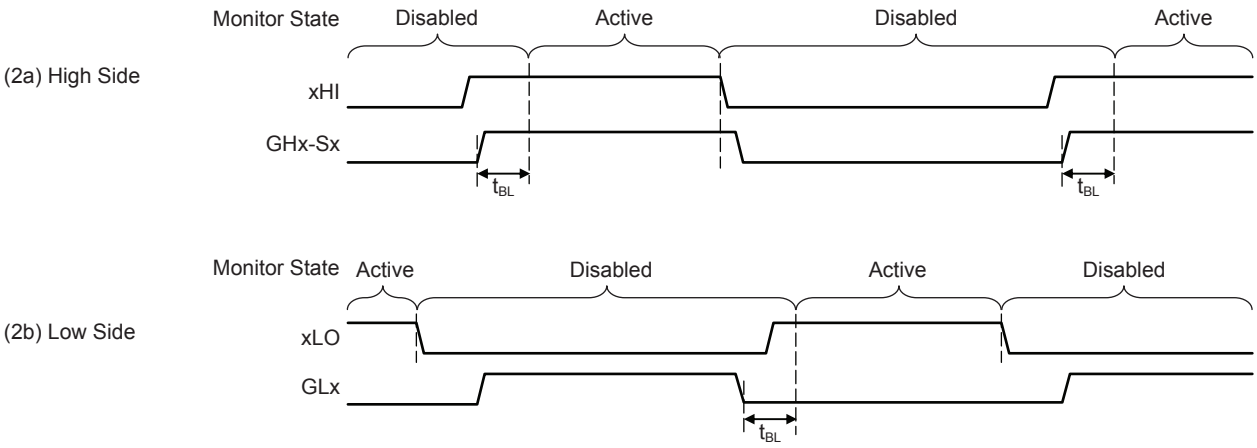


Figure 2. V_{DS} Overvoltage Internal Monitor Timing

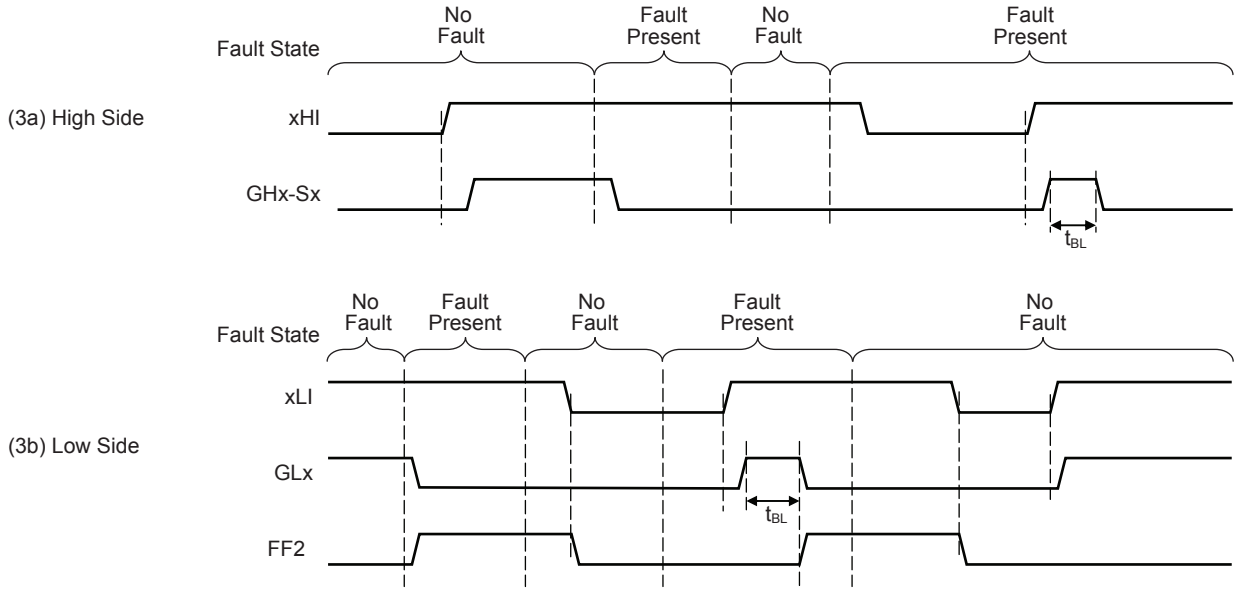


Figure 3. V_{DS} Overvoltage Fault Timing

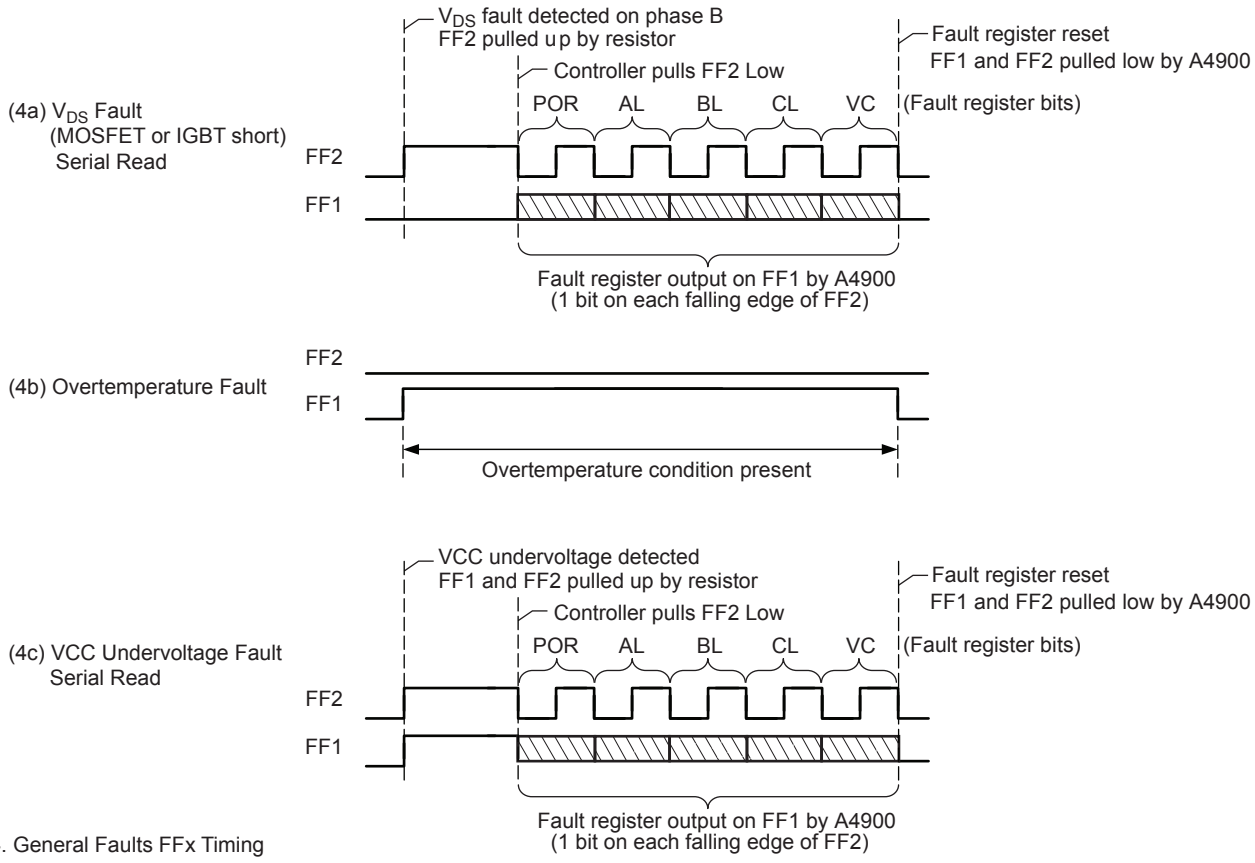


Figure 4. General Faults FFx Timing

Table 1. Phase Control Truth Table

Inputs				Outputs		Phase*	Comment
RESETn	COASTn	xHI	xLO	GHx	GLx	Sx	
0	x	x	x	L→Z	L→Z	Z	Low power shutdown
1	0	x	x	L→Z	L	Z	Coast
1	x	0	0	L	L	Z	Phase disabled
1	1	0	1	L	H	LO	Phase sinking
1	1	1	0	H	L	HI	Phase sourcing
1	x	1	1	L	L	Z	Phase disabled

Note: x = don't care, Z = high impedance, both switches off
*Phase HI = high-side switch (MOSFET or IGBT) active, Phase LO = low-side switch active

Table 2: Fault Definition

Fault Flags		Fault	Action Taken*
FF1	FF2		
0	0	No fault	No action
0	0	Bootstrap undervoltage	Disable switch
0	0	High-side V_{DS} overvoltage	Disable switch
0	1	Low-side V_{DS} overvoltage	Disable switch
1	0	Overtemperature	ESF = 0, No action ESF = 1, Disable all
1	1	Internal V_{DD} undervoltage	Disable all
1	1	VCC undervoltage	Disable all

*Disable Switch = turn off active power switching device (MOSFET or IGBT),
Disable All = turn off all power switching devices

Table 3: Fault Register Bit Definition

Bit	Sequence	Function
POR	1	Power-on-reset since last read
AL	2	V_{DS} exceeded on A phase low-side switch
BL	3	V_{DS} exceeded on B phase low-side switch
CL	4	V_{DS} exceeded on C phase low-side switch
VC	5	Undervoltage detected on VCC

Functional Description

The A4900 provides six gate drives, capable of driving a wide range of N-channel IGBT or power MOSFET switches. The gate drives are configured as three high-voltage high-side drives and three low-side drives. The high-side drives are isolated up to 600 V to allow operation with high bridge (motor) supply voltages. High-side drives use a bootstrap capacitor to provide the necessary gate drive voltage above the motor supply voltage. Each drive can be controlled with a TTL logic level input compatible with 3.3 V or 5 V logic systems.

A single supply input provides the gate drive supply and the bootstrap capacitor charge source. An internal regulator from the single supply provides the lower internal voltage for the logic circuit. The A4900 provides internal monitors to ensure that the gate-source voltage of both high-side and low-side external MOSFETs or IGBTs are above 9 V when active.

The control inputs to the A4900 provide a very flexible solution for many motor control applications. Each driver can be driven with an independent PWM signal allowing implementation of all motor excitation methods including trapezoidal and sinusoidal drive.

Diagnostics include short detection for the power switching devices, undervoltage detection for the key internal and external supplies and overtemperature detection. Two fault flags indicate three sets of faults and specific faults can be determined by reading a serial register.

Specific functions are described more fully in the following sections.

Terminal Functions

VCC Power supply for internal regulators and gate drive circuits. This supply also provides the charging source for the external bootstrap diodes. It should be decoupled with ceramic capacitors connected close to the VCC and GND terminals.

GND Power, digital, and reference ground. Low-side return path for discharge of the capacitance on the MOSFET or IGBT gates.

DHA, DHB, DHC High-side drain voltage sense input to the high-side V_{DS} monitors. Typically connected to the drain via a resistor potential divider.

BCA, BCB, BCC High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHA, GHB, GHC High-side, gate drive outputs for external N-channel MOSFETs or IGBTs.

SA, SB, SC Motor phase connections that are the negative supply connections for the floating high-side drivers and returns for the high-side gate discharge current to the sources of the high-side switches. They also are connected to the negative side of the bootstrap capacitors and provide the reference offset voltage for the high-side V_{DS} monitors.

DLA, DLB, DLC Low-side drain voltage sense input to the low-side V_{DS} monitors. Typically connected to the drain via a resistor potential divider.

GLA, GLB, GLC Low-side gate drive outputs for external N-channel MOSFETs or IGBTs.

AHI, ALO Logic inputs for phase A gate drive control.

BHI, BLO Logic inputs for phase B gate drive control.

CHI, CLO Logic inputs for phase C gate drive control.

COASTn Active-low logic input that forces all gate drive outputs low, and turns all external power switches off. Overrides all gate drive control inputs.

RESETn Active low logic input that resets faults when pulsed low. Allows low-power shutdown (sleep mode) when held low for more than the RESETn Shutdown Time, t_{RSD}.

FF1, FF2 Open drain fault flag outputs that indicate the presence of fault conditions. FF2 can be used as a clock input to read a serial register on FF1.

ESF Enable stop-on-fail logic input that determines actions to be taken during overtemperature fault conditions.

Power Supply

All internal supplies and references are derived from a single power supply connection to VCC at 15 V (typ). A single ground connection provides the return path for the operating current and the low-side gate discharge currents. The ground terminal must have a low impedance, low inductance path to the system ground of the main power bridge. The VCC supply must be decoupled with ceramic capacitors connected close to the supply and ground terminals. The supply for the internal logic is provided by an integrated linear regulator which provides the internal logic supply voltage, V_{DD}.

Gate Drive

The A4900 is designed to drive external, N-channel power switching devices, either MOSFET or IGBT. It supplies the transient currents necessary to quickly charge and discharge the external gate capacitance in order to reduce dissipation in the external power device during switching. The charge and discharge rate is controlled using an external resistor in series with the connection to the gate of the power switching device. In the following sections the letter *x* is used to represent the phase: A, B or C.

High-side gate drive

The floating high-side gate drive outputs at the GHA, GHB, and GHC terminals are referenced to the voltage at the respective SA, SB, or SC terminal. An external resistor between the gate drive output and the gate connection to the power switching device controls the slew rate seen at the gate, thereby providing some control of the di/dt in the bridge and the dv/dt of the Sx terminal. GHx = 1 (high) means that the upper half of the driver is turned on and the drain sources current to the gate of the high-side switching device in the external bridge, turning it on. GHx = 0 (low) means that the lower half of the driver is turned on and the drain sinks current from the gate of the external high-side switching device to the respective Sx terminal, turning it off.

When power is removed, a passive pull-down resistor between the GHx terminal and the corresponding Sx terminal ensures that the high-side switching device is held in the off state.

Bootstrap capacitors

The positive supply for the high-side gate driver on each phase is provided by a bootstrap capacitor, connected between the BCA and SA, BCB and SB, and BCC and SC terminals respectively. An external diode between the VCC terminal and each bootstrap capacitor is required to charge the capacitor when the associated output Sx terminal is low. The bootstrap capacitor is charged to approximately $V_{CC} - V_f$, where V_{CC} is the supply voltage at the VCC terminal and V_f is the forward voltage of the external blocking diode.

When the high-side switch is turned on, the voltage at the Sx terminal rises. This pushes the voltage at the other end of the bootstrap capacitor above V_{CC} and the diode stops current flowing from the bootstrap capacitor back to the VCC supply. The diode must have a reverse breakdown rating in excess of the bridge supply voltage because the voltage at the BCx terminal will be above the bridge voltage when the respective high-side switch is turned on.

After applying power or coming out of sleep mode, all three bootstrap capacitors must be charged before turning on any high-side switch. The capacitors can be charged by first turning on the three low-side switches for a short time. This will pull the Sx terminals low and allow the bootstrap diodes to apply a charging voltage across the capacitors.

Low-side gate drive

The low-side gate drive outputs at the GLA, GLB, and GLC terminals are referenced to the voltage at the GND terminal. An external resistor between the gate drive output and the gate connection to the power switching device controls the slew rate seen at the gate, thereby providing some control of the di/dt in the bridge and the dv/dt of the Sx terminal. GLx = 1 (high) means that the upper half of the driver is turned on and the drain sources current to the gate of the low-side power switching device in the external power bridge, turning it on. GLx = 0 (low) means that the lower half of the driver is turned on and the drain sinks current from the gate of the external low-side power switching device to the GND terminal, turning it off.

When power is removed, a passive pull-down resistor between the GLx terminal and the GND terminal ensures that the low-side switching device is held in the off state.

Logic Control Inputs

There are seven logic inputs that directly control the bridge. Two additional inputs provide systems and diagnostic management. All logic inputs are TTL compatible to allow operation with 3.3 V and 5 V logic. All inputs have a hysteresis of 300 mV (typ) to improve noise performance and an internal pull-down resistor of 50 kΩ (typ) to ensure that the outputs are disabled if the input control signals are removed.

Phase control

Each phase is controlled independently with two control inputs for each phase. The xHI input controls the high-side drive and the xLO input controls the low-side drive. Internal lock-out logic ensures that the high-side output drive and low-side output drive cannot be active simultaneously. Table 1 shows the logic truth table.

All gate drive outputs, GHx and GLx, can be forced low together by taking the COASTn input low. This turns all external power switching devices off and quickly disables the bridge in the event of a fault. COASTn does not clear any faults, so that the fault flags can be decoded and the serial fault word can be read. Because COASTn turns off all the external power switching

devices, it can also be used to provide fast decay PWM without synchronous rectification. If COASTn is held low, the high-side bootstrap capacitor may eventually become discharged and the high-side gate drive will then stop driving low. The high-impedance passive pull-down between the gate drive output and the corresponding source connection will then provide a discharge path to keep the high-side switch turned off. The low-side drive will remain active holding the low-side switch off.

Sleep mode and reset

When RESETn is held low for longer than the RESETn Shutdown Time, t_{RSD}, all gate drive outputs will initially be driven low. After a period of time determined by the charge state and value of the bootstrap capacitor, the high-side gate drive will stop driving. The high-impedance passive pull-down between the high-side gate drive output and the corresponding source connection will then provide a discharge path to keep the high-side switch turned off. The low-side drive will drive low for the Reset Hold-Off Delay Time, t_{RHD}, then stop driving. The high-impedance passive pull-down between the low-side gate drive output and the ground connection will then provide a discharge path to keep the low-side switch turned off.

The regulator and all internal circuitry are then disabled and the A4900 enters sleep mode. In sleep mode the current consumption from the VCC supply is reduced to the minimum level, and the latched faults and corresponding fault flags are cleared. When coming out of sleep mode the protection logic ensures that the gate drive outputs are off until the internal regulators reach their correct operating conditions.

When coming out of sleep mode all bootstrap capacitors must be charged before turning on any high-side switch, by first turning on the three low-side switches for a short time.

RESETn can also be used to clear any faults in the Fault register, without entering sleep mode, by taking it low for the RESETn Pulse Time, t_{RES}.

Diagnostics

Several diagnostic features are integrated into the A4900 to provide indication of fault conditions. In addition to system wide faults such as undervoltage and overtemperature, the A4900 integrates individual voltage monitors for each external power switching device. These are used to detect an overvoltage across the switching device when it is active, and to provide short circuit detection and protection.

Fault conditions are indicated by the states of the two open drain output fault flags, FF1 and FF2, as shown in table 2. In the event that two or more faults are detected simultaneously, the states of the fault flags are determined by a logical OR of the fault state of each flag.

When an undervoltage fault or a low-side switch overvoltage is detected, detailed fault information can be read from the fault outputs as a serial data word. When FF2 is high, a clock can be applied to FF2 and detailed fault information can be read from FF1 as a serial word. This can be used to determine on which of the three low-side external switching devices an overvoltage has been detected, or if a power-on reset or supply undervoltage has occurred. Fault register serial access operation is detailed in the Fault Register Serial Access section below.

The state of the enable stop-on-fault logic input, ESF, determines the action taken when an overtemperature fault is detected. For other fault conditions the action is defined by the type of fault, as shown in table 2.

Low-side switch overvoltage faults cause the fault flags and the relevant bit in the Fault register to be latched. For undervoltage faults the relevant bit in the Fault register is latched, but the flags are active only when the fault is present. For overtemperature faults the flags are active only when the fault is present.

Fault States

In addition to temperature, there are five voltage levels monitored in the A4900: the main supply voltage, the internally regulated logic supply voltage, and the voltage on each of the three high-side bootstrap capacitors.

Overtemperature

If the junction temperature exceeds the limit, 170°C (typ), FF1 goes high. When an overtemperature is detected, and ESF is high, the outputs are disabled automatically. If ESF is low, then no circuitry is disabled and the external controller must turn the outputs off or limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation. The overtemperature fault condition and the fault flags will be cleared only when the temperature drops below the recovery level, defined by $T_{JF} - T_{JHyst}$. Note that an overtemperature fault does not permit access to the Fault register, because FF2 remains low.

VCC undervoltage

VCC is the supply for the low-side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are sufficiently high before enabling any of the outputs. The undervoltage monitor circuit is active during power up. Both fault flags are high and the motor is coasting (all gate drives low) until V_{CC} is greater than approximately 11 V.

When a VCC undervoltage is detected, the fault flags and the fault register will be set and all gate drive outputs will be pulled low. When the VCC undervoltage condition is removed, the flags will be cleared and the outputs enabled. The VC bit in the Fault register will remain set until cleared by a register reset (see Fault Register Serial Access section, below).

Bootstrap undervoltage

The A4900 has three independent bootstrap voltage monitors, one for each phase. These monitor the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive voltage. Each phase operates independently, such that a bootstrap undervoltage on one phase does not affect the other two phases.

Before a high-side drive can be turned on, the voltage of the corresponding bootstrap capacitor must be higher than the turn-on voltage limit, V_{BCUVon}. If the bootstrap capacitor voltage is not above V_{BCUVon}, the A4900 does not allow the high-side gate drive output to go high.

The bootstrap voltage monitor for a phase remains active while a high-side gate drive output for that phase is commanded to be in the on state. If a high-side gate drive is high and the voltage of the corresponding bootstrap capacitor drops below the turn-off voltage, $V_{BCUVoff}$, then that high-side gate drive will be turned off. The output will remain off until an off-to-on transition is commanded by the control logic and the bootstrap capacitor voltage is above the turn-on voltage, V_{BCUVon}.

The bootstrap undervoltage fault state has no effect on the fault flag outputs or the Fault register.

V_{DD} undervoltage

The internal logic supply voltage, V_{DD}, is monitored to ensure correct logical operation. If an undervoltage of V_{DD} is detected, then the state of other reported faults might not be valid, so all fault states, fault flags, and the Fault register are reset and replaced by the V_{DD} undervoltage condition, and the outputs are disabled. When the V_{DD} undervoltage condition is removed all flags will be cleared and the outputs will be enabled.

V_{DS} overvoltage

Each of the six external power switching devices is provided with an independent overvoltage monitor, used to switch the device off if an overvoltage is detected. For each high-side power switching device, the monitor compares a fixed threshold voltage, V_{DSTH}, to the differential voltage between the DHx terminal and the Sx terminal. For each low-side power switching device, the monitor compares V_{DSTH} to the voltage between the DLx terminal and the GND terminal. The output of the monitor comparator is high when the monitored voltage is greater than V_{DSTH}, but is only valid when the associated switching device is turned on.

Power MOSFETs and IGBTs take a finite time to reach their full conduction state, so the monitored voltage may remain above the threshold and show a fault as the power switching device is turned on. To overcome this and avoid false short fault detection, the output of a comparator is ignored until one V_{DS} fault blank time, t_{BL}, after the associated external switching device is turned on. If the monitored voltage remains above V_{DSTH} after the V_{DS} fault blank time, then a short fault will be detected.

The monitored voltage is derived from the actual voltage across the power switching device using a resistor divider. This is necessary to prevent damage to the monitor input, either DHx or DLx, by the large differential voltage across the power switching device when the it is off. The monitor input is clamped to the respective reference point with a 5 V clamp. For the high-side the clamps are between the DHx and Sx terminals. For the low-side the clamps are between the DLx and GND terminals. The values of the resistors in the monitor voltage divider must be selected to ensure that the current through the clamp is limited to less than the maximum value, I_{DCL}. For example, a motor supply of 400 V means that the maximum voltage across the upper resistor in the divider will be 395 V. The current through the resistor must be less than 1 mA, so the resistor must be greater than 395 kΩ. If the required detection voltage across the power switching device is say 3 V, then the lower resistor in the divider must be 790 kΩ to achieve a monitor voltage of 2 V.

A short fault on either the high-side or the low-side always turns off the external switching device where the fault is detected, and holds it off until the control input is switched low then high again. This ensures that the overcurrent stress on the switching device is limited to a few microseconds after it is switched on.

Only the low-side V_{DS} overvoltage fault is indicated by the fault flags and captured in the Fault register. When a low-side fault is

present, the FF2 output is high and the associated (xL) bit in the Fault register is set. The FF2 output will remain high until reset. There are four ways the FF2 flag can be reset, assuming that the fault condition has been removed:

- Taking or pulsing RESETn low
- Taking the associated control input low
- A serial read
- A power on reset

It is possible to disable the V_{DS} overvoltage monitors by connecting the monitor input directly to its reference node (Sx or GND). This ensures that the monitor voltage is always zero so a fault is never detected.

Any low-side V_{DS} overvoltage fault always is latched in the Fault register until RESETn is low or a serial read is completed. (An undervoltage on the internal logic supply also will completely reset the short fault condition and the Fault register and replace it with a V_{DD} undervoltage fault.)

Fault Register Serial Access

The fault flag outputs, FF1 and FF2, are open drain and passively pulled high when a fault has been detected. This makes it possible to allow one or both of these fault pins to be driven externally to a logic low during a fault condition, when the A4900 is not pulling the fault pin low. One of these fault flags, FF2, can be used as a clock input to shift out the status of the Fault register, bit by bit, on the other fault flag FF1. When FF2 is pulled low by the A4900, either when no fault has been detected or when only an overtemperature fault is present, then no serial access is possible. The Fault register can be accessed only when FF2 goes high. This occurs when a low-side V_{DS} overvoltage, or a VCC or V_{DD} undervoltage, fault has been detected (see table 2).

Serial access method

FF1 and FF2 are monitored by the external controller. If FF2 goes high and FF1 remains low, then a low-side V_{DS} overvoltage has been detected. If FF1 and FF2 go high together, then a VCC or V_{DD} undervoltage has been detected.

In either case the A4900 response sequence will be:

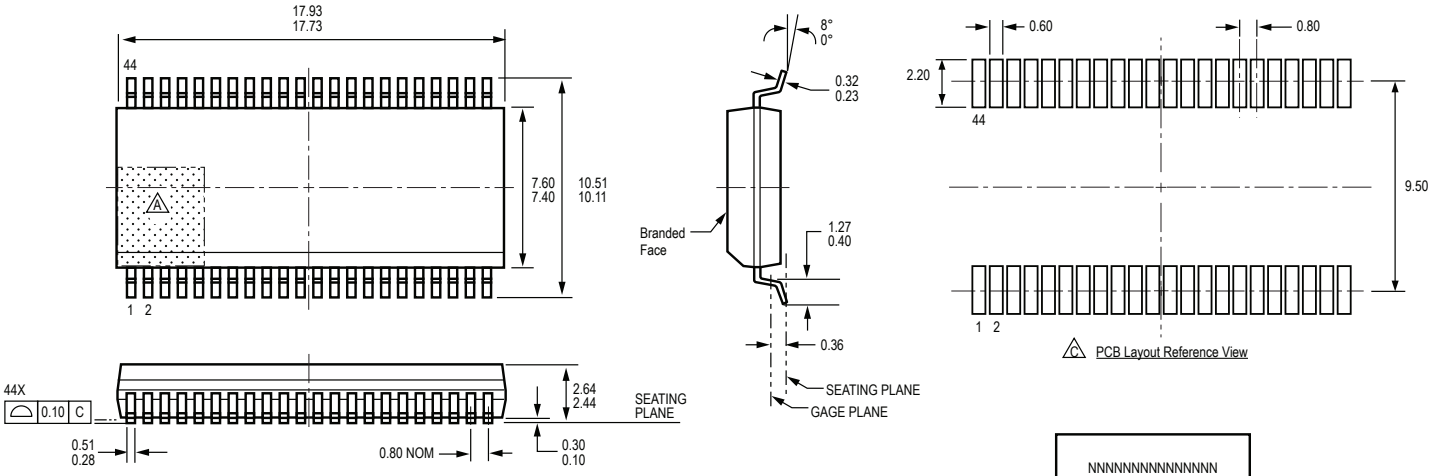
1. External controller takes any necessary additional action to protect the external MOSFETs or IGBTs.
2. Controller pulls FF2 low. A4900 responds by outputting the first bit of the Fault register, POR, on FF1.
3. Controller reads the fault bit and toggles FF2 high then low to request the next bit, AL. This continues for each of the 5 bits in the Fault register.
4. After the final bit, VC, is output on FF1, the controller takes FF2 high then low once more. Assuming that no fault conditions are present, the A4900 resets the Fault register and pulls FF1 and FF2 low to indicate no fault present.
5. Controller releases FF2.

The basic sequences for the three possible states of FF1 and FF2 are shown in figure 4.

At the end of the serial transfer, on the last high to low transition input to FF2, the Fault register and the fault flags are reset. However it is possible that one of the three unlatched fault conditions, VCC undervoltage, V_{DD} undervoltage, or overtemperature, is still present. In this case the fault flags will immediately show the fault status.

If a V_{DD} undervoltage occurs then both fault flags will be high, the POR bit will be set, and the remaining bits in the Fault register will be reset.

Package LQ, 44-Pin QSOP

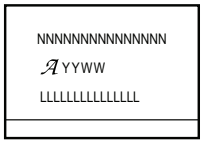


For Reference Only; not for tooling use (QSOP, nonJEDEC standard)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout (reference IPC7351 SOP80P1034X264-44M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)



B Standard Branding Reference View

N = Device part number
= Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot identifier

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