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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68030

ELECTRICAL SPECIFICATIONS

MOTOROLA

Rev 1

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.5 to +7.0	V
Operating Temperature Range			°C
Minimum Ambient Temperature	T_A	0	
40-MHz Maximum Ambient Temperature	T_A	70	
50-MHz Maximum Case Temperature	T_C	80	
Storage Temperature Range	T_{stg}	−55 to 150	°C

*A continuous clock must be supplied to the MC68030 when it is powered up.

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS — PGA PACKAGE

Characteristic	Symbol	Value	Rating
Thermal Resistance — Ceramic			°C/W
Junction to Ambient	θ_{JA}	30*	
Junction to Case	θ_{JC}	15*	

*Estimated

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected):

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

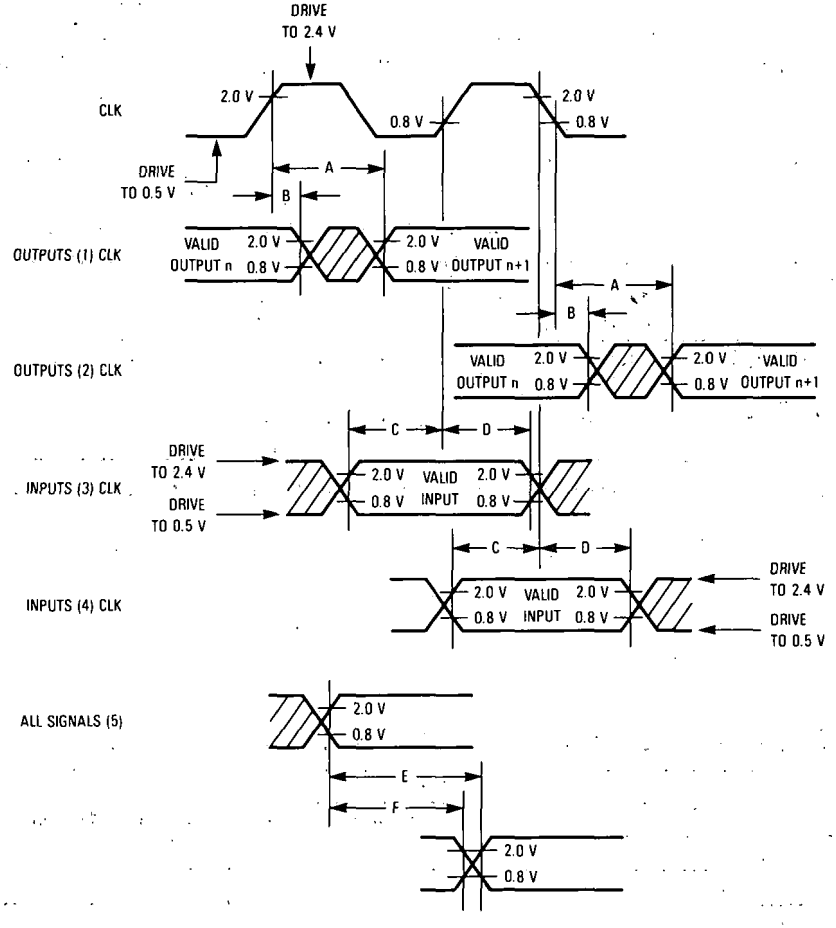
Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices," and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

AC ELECTRICAL SPECIFICATIONS DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the MC68030 clock input and, possibly, relative to one or more other signals.

The measurement of the AC specifications is defined by the waveforms in Figure 1. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in Figure 1. Outputs of the MC68030 are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs to the MC68030 are specified with minimum and, as appropriate, maximum setup and hold times, and are measured as shown. Finally, the measurements for signal-to-signal specifications are also shown.

Note that the testing levels used to verify conformance of the MC68030 to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:
1 - This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2 - This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3 - This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4 - *This input timing is applicable to all parameters specified relative to the falling edge of the clock.*
5 - This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A - Maximum output delay specification
B - Minimum output hold time
C - Minimum input setup time specification
D - Minimum input hold time specification
E - Signal valid to signal valid specification (maximum or minimum)
F - Signal valid to signal invalid specification (maximum or minimum)

Figure 1. Drive Levels and Test Points for AC Specifications

DC ELECTRICAL SPECIFICATIONS

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; 40 MHz-T_A = 0° to 70°C, 50 MHz-T_A = 0°C to T_C = 80°C)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND −0.5	0.8	V
Input Leakage Current GND ≤ V_{in} ≤ V_{CC}	$\overline{BERR}$, $\overline{BR}$, $\overline{BGACK}$, CLK, $\overline{IPL0}$–$\overline{IPL2}$, $\overline{AVEC}$, $\overline{CDIS}$, $\overline{DSACK0}$, $\overline{DSACK1}$	I_{in}	−2.5	2.5	μA
	$\overline{HALT}$, $\overline{RESET}$		−20	20	
Hi-Z (Off-State) Leakage Current @ 2.4 V/0.5 V	A0–A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0–D31, FC0–FC2, R/$\overline{W}$, $\overline{RMC}$, SIZ0–SIZ1	I_{TSI}	−20	20	μA
Output High Voltage I_{OH} = 400 μA	A0–A31, $\overline{AS}$, $\overline{BG}$, D0–D31, $\overline{DBEN}$, $\overline{DS}$, $\overline{ECS}$, R/$\overline{W}$, $\overline{IPEND}$, $\overline{OCS}$, $\overline{RMC}$, SIZ0–SIZ1, FC0–FC2, $\overline{CBREQ}$, $\overline{CIOUT}$, $\overline{STATUS}$, $\overline{REFILL}$	V_{OH}	2.4	—	V
Output Low Voltage		V_{OL}			V
I_{OL} = 3.2 mA	A0–A31, FC0–FC2, SIZ0–SIZ1, $\overline{BG}$, D0–D31		—	0.5	
I_{OL} = 5.3 mA	$\overline{CBREQ}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{RMC}$, $\overline{DBEN}$, $\overline{IPEND}$		—	0.5	
I_{OL} = 2.0 mA	$\overline{STATUS}$, $\overline{REFILL}$, $\overline{CIOUT}$, $\overline{ECS}$, $\overline{OCS}$		—	0.5	
I_{OL} = 10.7 mA	$\overline{RESET}$		—	0.5	
Power Dissipation (T_A = 0°C)		P_D	—	2.6	W
Capacitance (see Note) V_{in} = 0 V, T_A = 25°C, f = 1 MHz		C_{in}	—	20	pF
Load Capacitance	$\overline{ECS}$, $\overline{OCS}$	C_L	—	50	pF
	$\overline{CIOUT}$, $\overline{STATUS}$, $\overline{REFILL}$			70	
	All Other			130	

NOTE: Capacitance is periodically sampled rather than 100% tested.

AC ELECTRICAL SPECIFICATIONS — CLOCK INPUT (see Figure 2)

Num.	Characteristic	20 MHz		25 MHz		33.33 MHz		40 MHz		50 MHz*		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of Operation	12.5	20	12.5	25	20	33.33	25	40	25	50	MHz
1	Cycle Time Clock	50	80	40	80	30	50	25	40	20	40	ns
2, 3	Clock Pulse Width Measured from 1.5 V to 1.5 V	23	57	19	61	14	36	11.5	29	9.5	30.5	ns
4, 5	Clock Rise and Fall Times	—	5	—	4	—	3	—	2	—	2	ns

*T_{case} = 80°C Maximum

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ±5%; GND = 0 Vdc; 40 MHz-T_A = 0° to 70°C, 50 MHz-T_A = 0°C to T_C = 80°C)
(see Figures 3–8)

Num.	Characteristic	20 MHz		25 MHz		33.33 MHz		40 MHz		50 MHz*		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
6	Clock High to Function Code, Size, RMC, IPEND, CIOUT, Address Valid	0	25	0	20	0	14	0	14	0	14	ns
6A	Clock High to ECS, OCS Asserted	0	15	0	15	0	12	0	10	0	10	ns
6B	Function Code, Size, RMC, IPEND, CIOUT, Address Valid to Negating Edge of ECS	4	—	3	—	3	—	3	—	3	—	ns
7	Clock High to Function Code, Size, RMC, CIOUT, Address, Data High Impedance	0	50	0	40	0	30	0	25	0	20	ns
8	Clock High to Function Code, Size, RMC, IPEND, CIOUT, Address Invalid	0	—	0	—	0	—	0	—	0	—	ns
9	Clock Low to AS, DS Asserted, CBREQ Valid	3	20	3	18	2	10	2	10	2	10	ns
9A[1]	AS to DS Assertion Skew (Read)	−10	10	−10	10	−8	8	−6	6	−6	6	ns
9B[14]	AS Asserted to DS Asserted (Write)	32	—	27	—	22	—	16	—	14	—	ns
10	ECS Width Asserted	15	—	10	—	8	—	5	—	4	—	ns
10A	OCS Width Asserted	15	—	10	—	8	—	5	—	4	—	ns
10B[7]	ECS, OCS Width Negated	10	—	5	—	5	—	5	—	4	—	ns
11	Function Code, Size, RMC, CIOUT, Address Valid to Asserting Edge of AS Asserted (and DS Asserted, Read)	10	—	7	—	5	—	5	—	3	—	ns
12	Clock Low to AS, DS, CBREQ Negated	0	20	0	18	0	10	0	10	0	10	ns
12A	Clock Low to ECS/OCS Negated	0	20	0	18	0	15	0	12	0	11	ns
13	AS, DS Negated to Function Code, Size, RMC, CIOUT, Address Invalid	10	—	7	—	5	—	3	—	3	—	ns
14	AS (and DS Read) Width Asserted (Asynchronous Cycle)	85	—	70	—	45	—	30	—	25	—	ns
14A[11]	DS Width Asserted (Write)	38	—	30	—	23	—	18	—	13	—	ns
14B	AS (and DS, Read) Width Asserted (Synchronous Cycle)	35	—	30	—	23	—	18	—	13	—	ns
15	AS, DS Width Negated	38	—	30	—	23	—	18	—	13	—	ns
15A[8]	DS Negated to AS Asserted	30	—	25	—	18	—	16	—	14	—	ns
16	Clock High to AS, DS, R/W, DBEN, CBREQ High Impedance	—	50	—	40	—	30	—	25	—	20	ns

AC ELECTRICAL SPECIFICATIONS (Continued)

Num.	Characteristic	20 MHz		25 MHz		33.33 MHz		40 MHz		50 MHz*		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	10	—	7	—	5	—	3	—	3	—	ns
18	Clock High to R/$\overline{W}$ High	0	25	0	20	0	15	0	14	0	14	ns
20	Clock High to R/$\overline{W}$ Low	0	25	0	20	0	15	0	14	0	14	ns
21	R/$\overline{W}$ High to $\overline{AS}$ Asserted	10	—	7	—	5	—	5	—	3	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	60	—	47	—	35	—	24	—	23	—	ns
23	Clock High to Data-Out Valid	—	25	—	20	—	14	—	14	—	14	ns
24	Data-Out Valid to Negating Edge of $\overline{AS}$	8	—	5	—	3	—	3	—	3	—	ns
25[11]	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid	10	—	7	—	5	—	3	—	3	—	ns
25A[9,11]	$\overline{DS}$ Negated to $\overline{DBEN}$ Negated (Write)	10	—	7	—	5	—	3	—	3	—	ns
26[11]	Data-Out Valid to Asserting Edge of $\overline{DS}$ Asserted (Write)	10	—	7	—	5	—	3	—	3	—	ns
27	Data-In Valid to Clock Low (Setup)	4	—	2	—	1	—	1	—	1	—	ns
27A	Late $\overline{BERR}$/$\overline{HALT}$ Asserted to Clock Low (Setup)	10	—	5	—	3	—	3	—	3	—	ns
28[12]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated (Asynchronous Hold)	0	50	0	40	0	30	0	20	0	15	ns
28A[12]	Clock Low to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated (Synchronous Hold)	12	85	8	70	6	50	6	40	6	35	ns
29[12]	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Asynchronous Hold)	0	—	0	—	0	—	0	—	0	—	ns
29A[12]	$\overline{AS}$, $\overline{DS}$ Negated to Data-In High Impedance	—	50	—	40	—	30	—	25	—	20	ns
30[12]	Clock Low to Data-In Invalid (Synchronous Hold)	12	—	8	—	6	—	6	—	6	—	ns
30A[12]	Clock Low to Data-In High Impedance (Read followed by Write)	—	75	—	60	—	45	—	30	—	25	ns
31[2]	$\overline{DSACKx}$ Asserted to Data-In Valid (Asynchronous Data Setup)	—	43	—	28	—	20	—	14	—	13	ns
31A[3]	$\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid (Skew)	—	10	—	7	—	5	—	3	—	3	ns
32	$\overline{RESET}$ Input Transition Time	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	Clks
33	Clock Low to $\overline{BG}$ Asserted	0	25	0	20	0	15	0	14	0	14	ns
34	Clock Low to $\overline{BG}$ Negated	0	25	0	20	0	15	0	14	0	14	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks

AC ELECTRICAL SPECIFICATIONS (Continued)

Num.	Characteristic	20 MHz		25 MHz		33.33 MHz		40 MHz		50 MHz*		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[6]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	0	1.5	0	1.5	0	1.5	0	1.5	0	1.5	Clks
39	$\overline{BG}$ Width Negated	75	—	60	—	45	—	30	—	30	—	ns
39A	$\overline{BG}$ Width Asserted	75	—	60	—	45	—	30	—	30	—	ns
40	Clock High to $\overline{DBEN}$ Asserted (Read)	0	25	0	20	0	18	0	16	0	14	ns
41	Clock Low to $\overline{DBEN}$ Negated (Read)	0	25	0	20	0	18	0	16	0	14	ns
42	Clock Low to $\overline{DBEN}$ Asserted (Write)	0	25	0	20	0	18	0	16	0	14	ns
43	Clock High to $\overline{DBEN}$ Negated (Write)	0	25	0	20	0	18	0	16	0	14	ns
44	R/$\overline{W}$ Low to $\overline{DBEN}$ Asserted (Write)	10	—	7	—	5	—	5	—	5	—	ns
45[5]	$\overline{DBEN}$ Width Asserted Asynchronous Read Asynchronous Write	50 100	— —	40 80	— —	30 60	— —	22 45	— —	20 40	— —	ns
45A[9]	$\overline{DBEN}$ Width Asserted Synchronous Read Synchronous Write	10 50	— —	5 40	— —	5 30	— —	5 22	— —	5 20	— —	ns
46	R/$\overline{W}$ Width Asserted (Asynchronous Write or Read)	125	—	100	—	75	—	50	—	40	—	ns
46A	R/$\overline{W}$ Width Asserted (Synchronous Write or Read)	75	—	60	—	45	—	30	—	25	—	ns
47A	Asynchronous Input Setup Time to Clock Low	4	—	2	—	2	—	2	—	2	—	ns
47B	Asynchronous Input Hold Time from Clock Low	12	—	8	—	6	—	6	—	6	—	ns
48[4]	$\overline{DSACKx}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	—	20	—	25	—	18	—	14	—	13	ns
53	Data-Out Hold from Clock High	3	—	3	—	2	—	2	—	2	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	25	—	20	—	15	—	11	—	11	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	512	—	512	—	512	—	512	—	512	—	Clks
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	0	—	0	—	0	—	0	—	0	—	ns
58[10]	$\overline{BGACK}$ Negated to Bus Driven	1	—	1	—	1	—	1	—	1	—	Clks
59[10]	$\overline{BG}$ Negated to Bus Driven	1	—	1	—	1	—	1	—	1	—	Clks

AC ELECTRICAL SPECIFICATIONS (Concluded)

Num.	Characteristic	20 MHz		25 MHz		33.33 MHz		40 MHz		50 MHz*		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
60[13]	Synchronous Input Valid to Clock High (Setup Time)	4	—	2	—	2	—	2	—	2	—	ns
61[13]	Clock High to Synchronous Input Invalid (Hold Time)	12	—	8	—	6	—	6	—	6	—	ns
62	Clock Low to $\overline{\text{STATUS}}$, $\overline{\text{REFILL}}$ Asserted	0	25	0	20	0	15	0	15	0	15	ns
63	Clock Low to $\overline{\text{STATUS}}$, $\overline{\text{REFILL}}$ Negated	0	25	0	20	0	15	0	15	0	15	ns

NOTES:
*T_{case} = 80°C Maximum

1. This number can be reduced to 5 ns if strobes have equal loads.
2. If the asynchronous setup time (#47A) requirements are satisfied, the $\overline{\text{DSACKx}}$ low to data setup time (#31) and $\overline{\text{DSACKx}}$ low to $\overline{\text{BERR}}$ low setup time (#48) can be ignored. The data must only satisfy the data-in clock low setup time (#27) for the following clock cycle, and $\overline{\text{BERR}}$ must only satisfy the late $\overline{\text{BERR}}$ low to clock low setup time (#27A) for the following clock cycle.
3. This parameter specifies the maximum allowable skew between $\overline{\text{DSACK0}}$ to $\overline{\text{DSACK1}}$ asserted or $\overline{\text{DSACK1}}$ to $\overline{\text{DSACK0}}$ asserted; specification #47A must be met by $\overline{\text{DSACK0}}$ or $\overline{\text{DSACK1}}$.
4. This specification applies to the first ($\overline{\text{DSACK0}}$ or $\overline{\text{DSACK1}}$) $\overline{\text{DSACKx}}$ signal asserted. In the absence of $\overline{\text{DSACKx}}$, $\overline{\text{BERR}}$ is an asynchronous input using the asynchronous input setup time (#47A).
5. $\overline{\text{DBEN}}$ may stay asserted on consecutive write cycles.
6. The minimum values must be met to guarantee proper operation. If this maximum value is exceeded, $\overline{\text{BG}}$ may be reasserted.
7. This specification indicates the minimum high time for $\overline{\text{ECS}}$ and $\overline{\text{OCS}}$ in the event of an internal cache hit followed immediately by another cache hit, a cache miss, or an operand cycle.
8. This specification guarantees operation with the MC68881/MC68882, which specifies a minimum time for $\overline{\text{DS}}$ negated to $\overline{\text{AS}}$ asserted (specification #13A in the *MC68881/MC68882 User's Manual*). Without this specification, incorrect interpretation of specifications #9A and #15 would indicate that the MC68030 does not meet the MC68881/MC68882 requirements.
9. This specification allows a system designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{\text{DBEN}}$. The timing on $\overline{\text{DBEN}}$ precludes its use for synchronous READ cycles with no wait states.
10. These specifications allow system designers to guarantee that an alternate bus master has stopped driving the bus when the MC68030 regains control of the bus after an arbitration sequence.
11. $\overline{\text{DS}}$ will not be asserted for synchronous write cycles with no wait states.
12. These hold times are specified with respect to strobes (asynchronous) and with respect to the clock (synchronous). The designer is free to use either time.
13. Synchronous inputs must meet specifications #60 and #61 with stable logic levels for ***all*** rising edges of the clock while $\overline{\text{AS}}$ is asserted. These values are specified relative to the high level of the rising clock edge. The values originally published were specified relative to the low level of the rising clock edge.
14. This specification allows system designers to qualify the $\overline{\text{CS}}$ signal of an MC68881/MC68882 with $\overline{\text{AS}}$ (allowing 7 ns for a gate delay) and still meet the $\overline{\text{CS}}$ to $\overline{\text{DS}}$ setup time requirement (spec 8B) of the MC68881/MC68882.

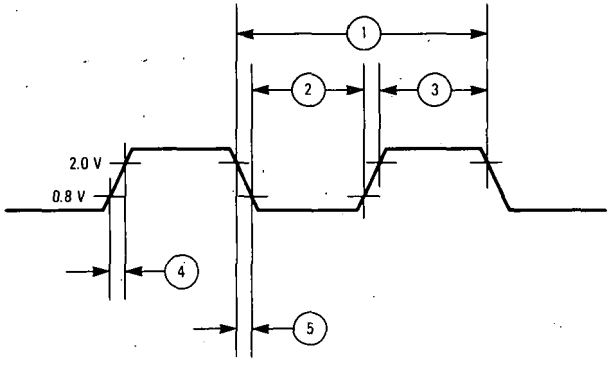


Figure 2. Clock Input Timing Diagram

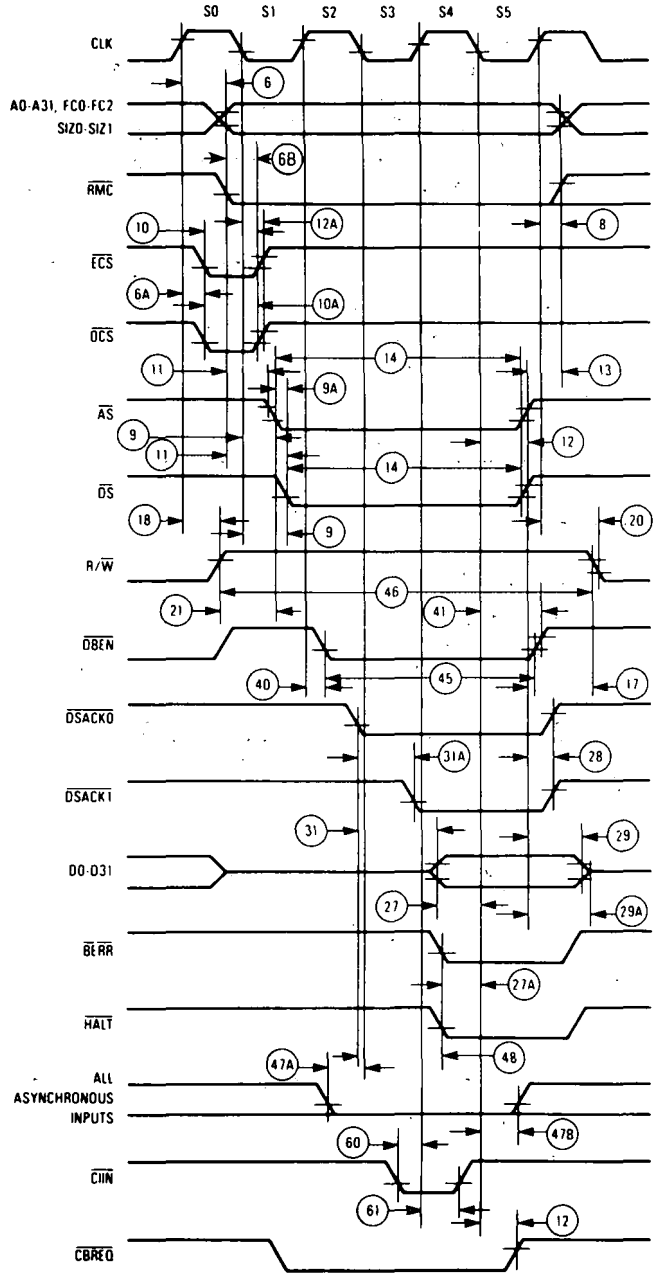


Figure 3. Asynchronous Read Cycle Timing Diagram

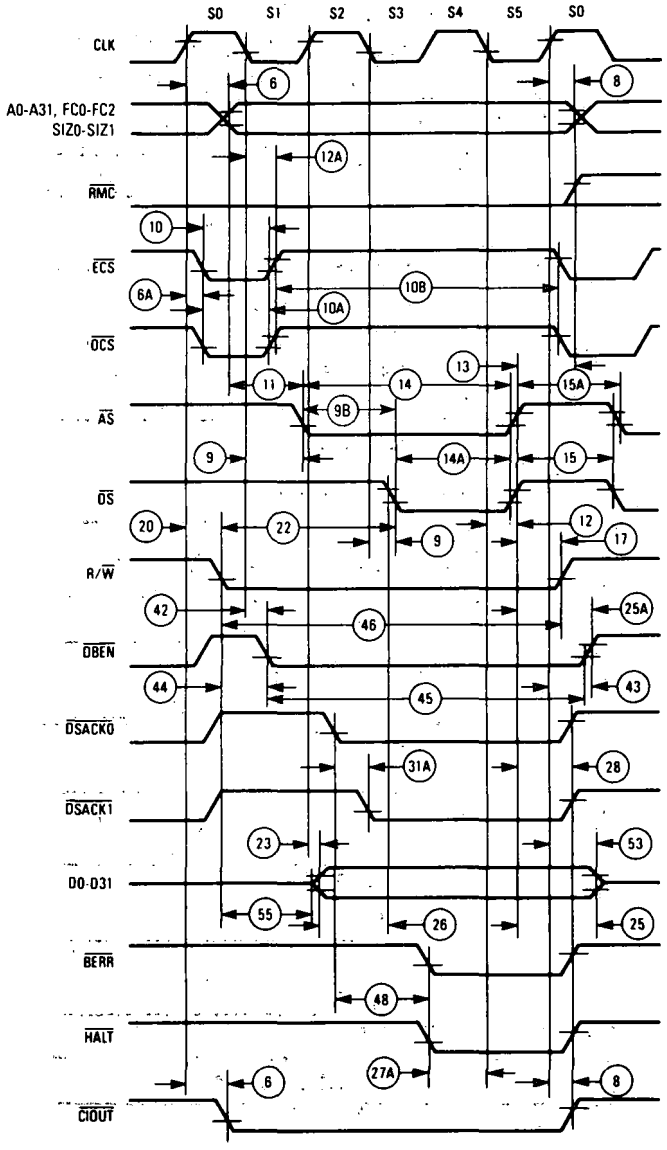


Figure 4. Asynchronous Write Cycle Timing Diagram

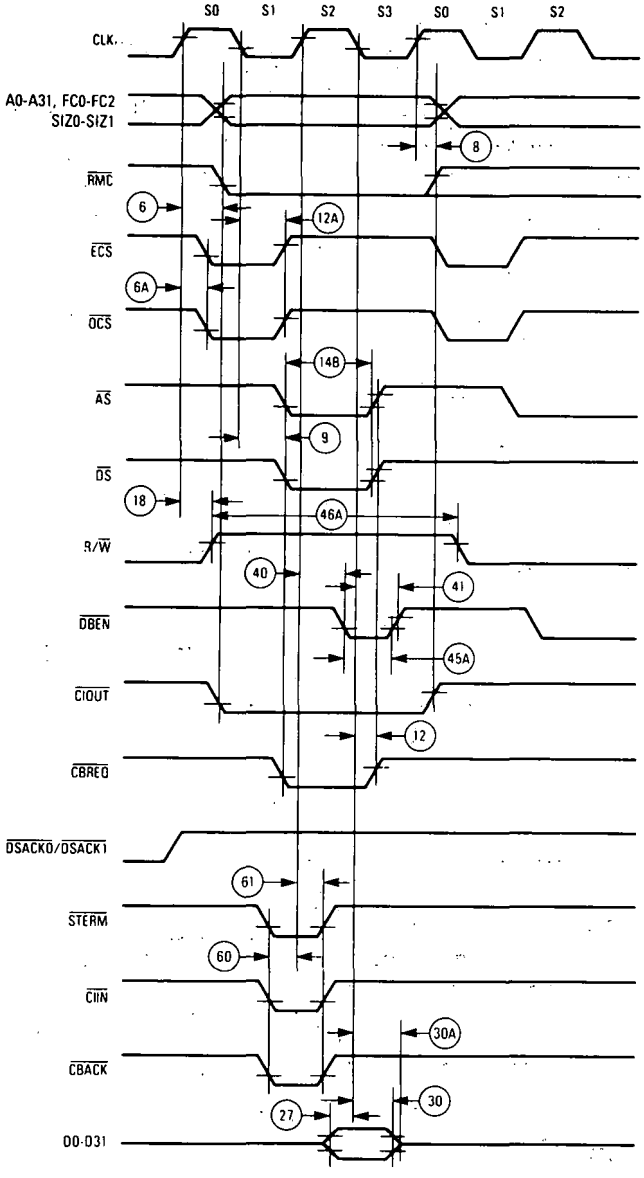


Figure 5. Synchronous Read Cycle Timing Diagram

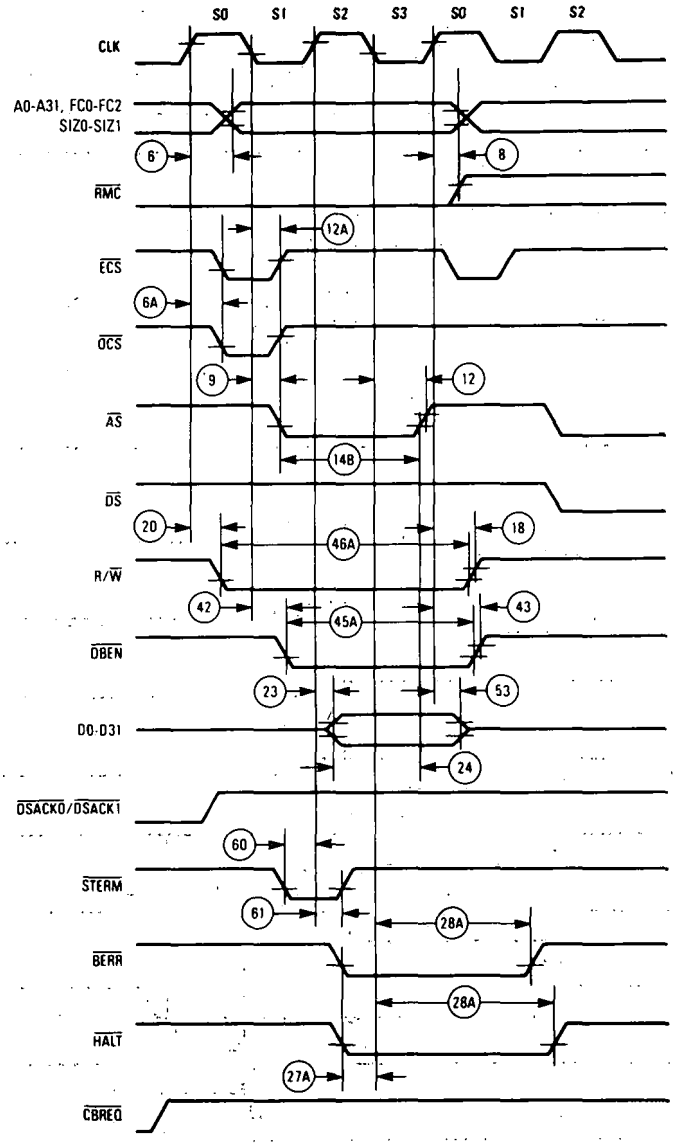


Figure 6. Synchronous Write Cycle Timing Diagram

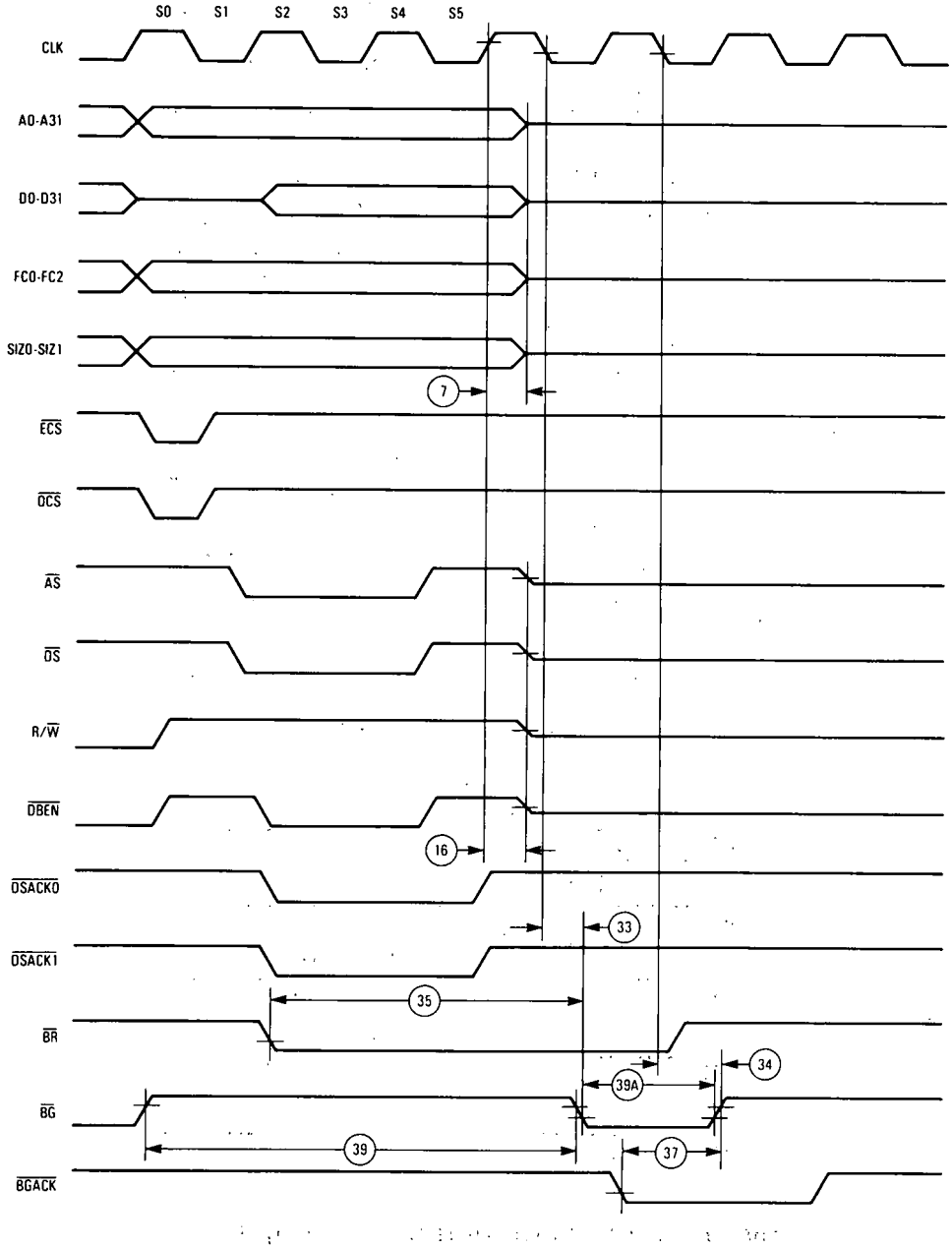


Figure 7. Bus Arbitration Timing Diagram

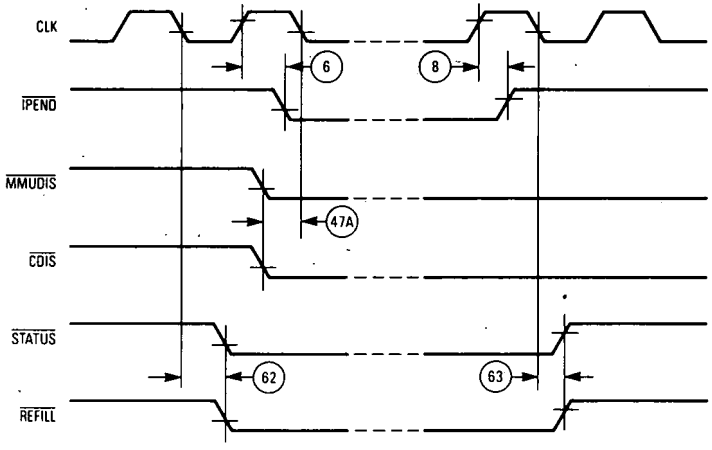


Figure 8. Other Signal Timings

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; P.O. Box 80300; Cheung Sha Wan Post Office; Kowloon Hong Kong.
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