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Contact information:

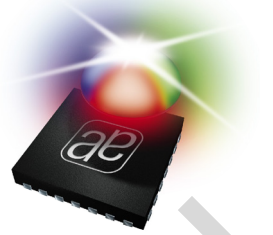
Headquarters:

ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at www.ams.com

AS3644

Ultra Small Low Cost 320mA Inductive White LED Flash Driver



1 General Description

The AS3644 is an inductive high efficient DCDC step up converter driving a current source. The DCDC step up converter operates at a fixed frequency of 4MHz and includes soft startup to allow easy integration into noise sensitive RF systems. The current source operates in flash/torch/assist (video/autofocus) mode.

The AS3644 includes flash timer, overvoltage, overtemperature, undervoltage and LED short circuit protection functions.

The AS3644 is able to detect a broken coil. Together with the LED short and open detection the AS3644 can be used to verify the connection to its external components and allowing in-circuit test. This reduces test time and simplifies production test procedures.

The AS3644 is controlled by an I²C interface to allow sophisticated control of all settings like currents and timings.

The complete flash driver solution measures only 11mm² PCB area.

The AS3644 is available in a space-saving WL-CSP package measuring only 1.5x1.1x0.6mm and operates over the -30°C to +85°C temperature range.

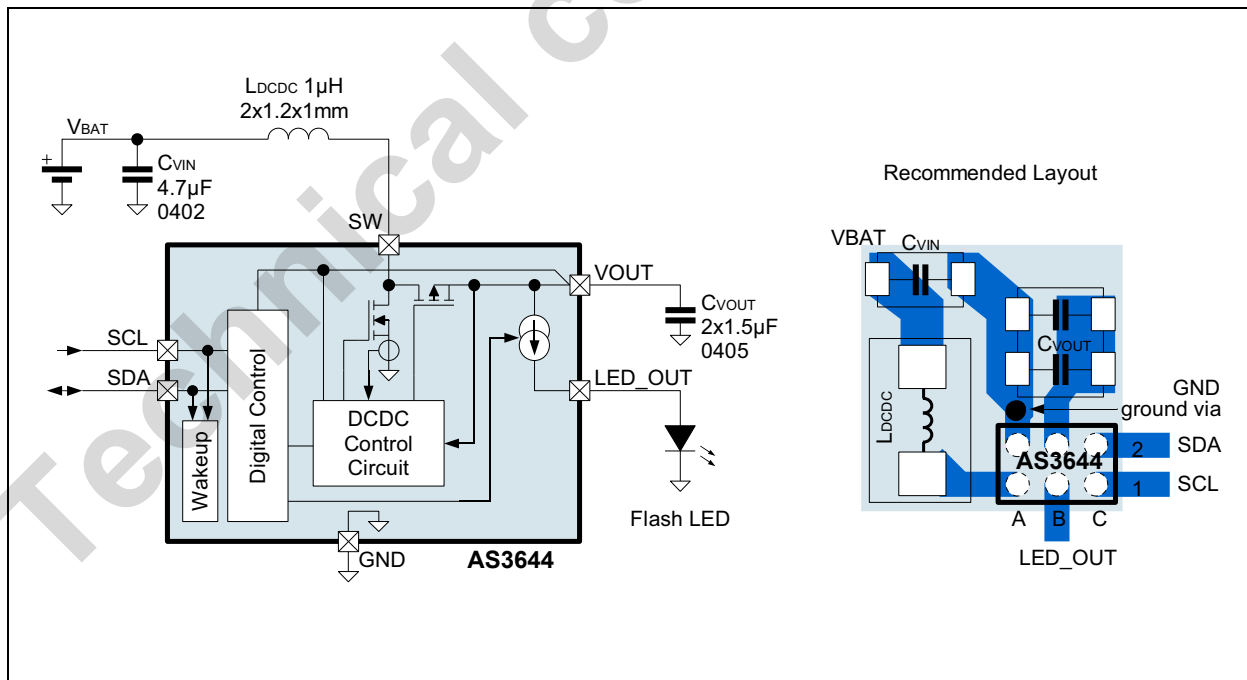
2 Key Features

- Total flash driver solution only 11mm²
- High efficiency 4MHz fixed frequency DCDC Boost converter with soft start allows small coils
- LED currents
260mA to 320mA flash current (20mA steps)
51.6mA or 72.3mA Assist light (=torch) current
- Flash LED(s) cathode connected to ground:
Improved thermal performance (ground = heat sink)
Simplified PCB layout
- Adjustable Flash Timer
30ms to 480ms in 30ms steps
- Flash, Torch, Assist and Indicator Mode
- Protection functions:
Automatic Flash timer to protect the LED
Overvoltage and undervoltage Protection
Overtemperature Protection
LED short circuit protection
- Available in tiny WL-CSP Packages
2x3 balls 0.5mm pitch, 1.5x1.1x0.6mm package size

3 Applications

Flash/Torch for mobile phones, digital cameras and PDA

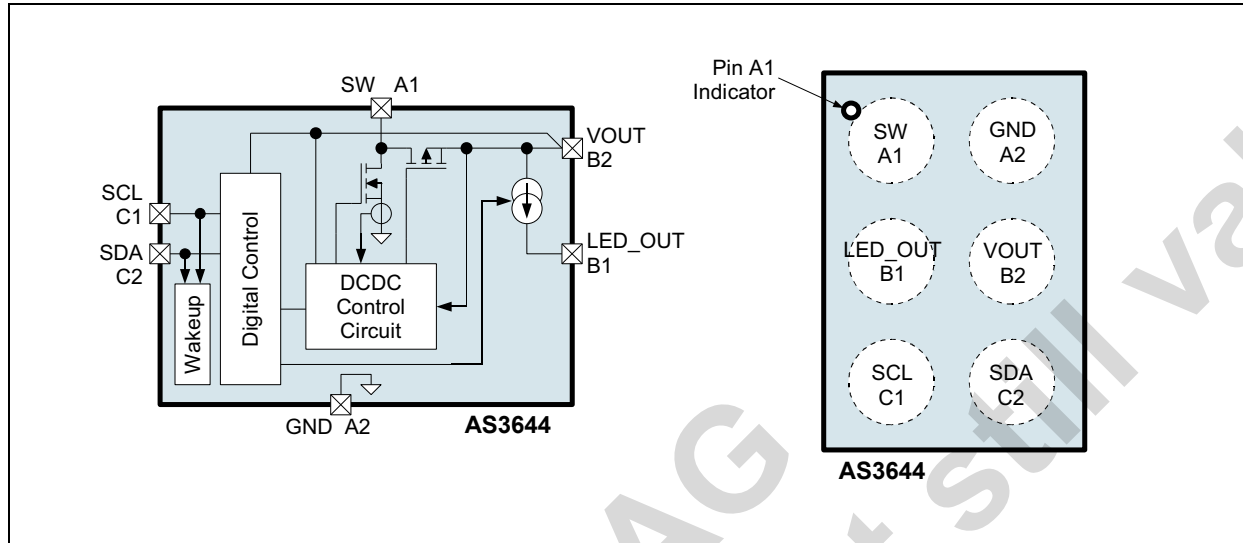
Figure 1. Typical Operating Circuit



4 Pinout

Pin Assignment

Figure 2. Pin Assignments (Top View)



Pin Description

Table 1. Pin Description for AS3644

Pin Number	Pin Name	Description
A1	SW	DCDC converter switching node - make a short connection to the coil L _{DCDC}
A2	GND	Power and signal ground - connect to GND and make a short connection to C _{VOUT}
B1	LED_OUT	Flash LED current source output
B2	VOUT	DCDC converter output capacitor and supply for AS3644 - make a short connection to C _{VOUT}
C1	SCL	serial clock input in I ² C interface
C2	SDA	serial data input/output for I ² C interface (needs external pullup resistor)

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Table 3](#), "Electrical Characteristics," on [page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VOUT, SW to GND	-0.3	+7.0	V	
SCL, SDA, LED_OUT to GND	-0.3	VOUT+ 0.3	V	max. +7V
VOUT to SW	-0.3		V	Note: Diode between VOUT and SW
Input Pin Current without causing latchup	-100	+100 +IIN	mA	Norm: EIA/JESD78
Continuous Power Dissipation (T_A = +70°C)				
Continuous power dissipation		530	mW	P _T ¹ at 70°C ambient
Continuous power dissipation derating factor		7.2	mW/°C	P _{DERATE} ²
Electrostatic Discharge				
ESD HBM		±2000	V	Norm: JEDEC JESD22-A114F
ESD CDM		±500	V	Norm: JEDEC JESD 22-C101C
ESD MM		±100	V	Norm: JEDEC JESD 22-A115-A level A
Temperature Ranges and Storage Conditions				
Junction Temperature		+150	°C	Internally limited (overtemperature protection) max. 20000s
Storage Temperature Range	-55	+125	°C	
Humidity	5	85	%	Non condensing
Body Temperature during Soldering		+260	°C	according to IPC/JEDEC J-STD-020

1. Depending on actual PCB layout and PCB used; for peak power dissipation during flashing see document 'AS3644 Thermal Measurements'
2. P_{DERATE} derating factor changes the total continuous power dissipation (P_T) if the ambient temperature is not 70°C. Therefore for e.g. T_{AMB}=85°C calculate P_T at 85°C = P_T - P_{DERATE} * (85°C - 70°C)

6 Electrical Characteristics

$V_{VIN} = +2.7V$ to $+5.5V$, $T_{AMB} = -30^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified. Typical values are at $V_{VIN} = +3.7V$, $T_{AMB} = +25^{\circ}C$, unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General Operating Conditions						
V_{VIN}	Supply Voltage		2.7	3.7	4.5	V
$V_{VINREDUCE_D_FUNC}$	Supply Voltage	AS3644 functionally working, but not all parameters fulfilled ¹	2.5		5.0	V
$I_{SHUTDOWN}$	Shutdown Current	$SCL=L$, $SDA=L$, $V_{VIN}<3.7V$, $0^{\circ}C < T_{AMB} < 50^{\circ}C$		0.5	1.0	μA
I_{STANBY}	Standby Current	interface active, $V_{VIN}<3.7V$		0.5	5	μA
T_{AMB}	Operating Temperature		-30	25	85	$^{\circ}C$
DCDC Step Up Converter						
V_{VOUT}	DCDC Boost output Voltage (pin VOUT)	For high supply voltages the output voltage can reach up to $V_{VOUTMAX}$ (the AS3644 always runs in PWM mode unless $V_{VOUT}>V_{VOUTMAX}$ or during startup)	2.8		4.7	V
η	Efficiency	$I_{LED_OUT}=300mA$, $V_{VOUT}=4.2V$		82		%
f_{CLK}	Operating Frequency	All internal timings are derived from this oscillator	-7.5%	4.0	+7.5%	MHz
		DCDC operating frequency for short pulses (close to 100% operating mode)	-7.5%	1.0	+7.5%	
Current Source						
I_{LED_OUT}	LED_OUT current source output		51.6		320	mA
$I_{LED_OUT\Delta}$	LED_OUT current source accuracy	$I_{LED_OUT}=300mA$ or $72.3mA$	-7		+7	%
$I_{LED_OUT_RAMP}$	LED_OUT ramp time at $I_{LED_OUT}=300mA$	Ramp-up During startup	0.6		1.0	ms
		Ramp-down after AS3644 is disabled by interface	0.2		0.7	ms
$I_{LED_OUT_RIPPLE}$	LED_OUT current ripple	$I_{LED_OUT} = 300mA$		10		mAPP
V_{ILED_COMP}	LED_OUT current source voltage compliance	Minimum voltage between pin VOUT and LED_OUT for operation of the current source		210	350	mV
Protection and Fault Detection Functions (see page 9)						
$V_{VOUTMAX}$	V_{VOUT} overvoltage protection	DCDC Converter Overvoltage Protection	5.0	5.25	5.5	V
I_{LIMIT}	Current Limit for coil LDCDC (Pin SW) measured at 50% PWM duty cycle ²	maximum 40000s lifetime operation in overcurrent limit	0.7	0.8	0.9	A
V_{LED_SHORT}	Flash LED short circuit detection voltage	Voltage measured on pin LED_OUT		1.45	1.65	V

Table 3. Electrical Characteristics (Continued)

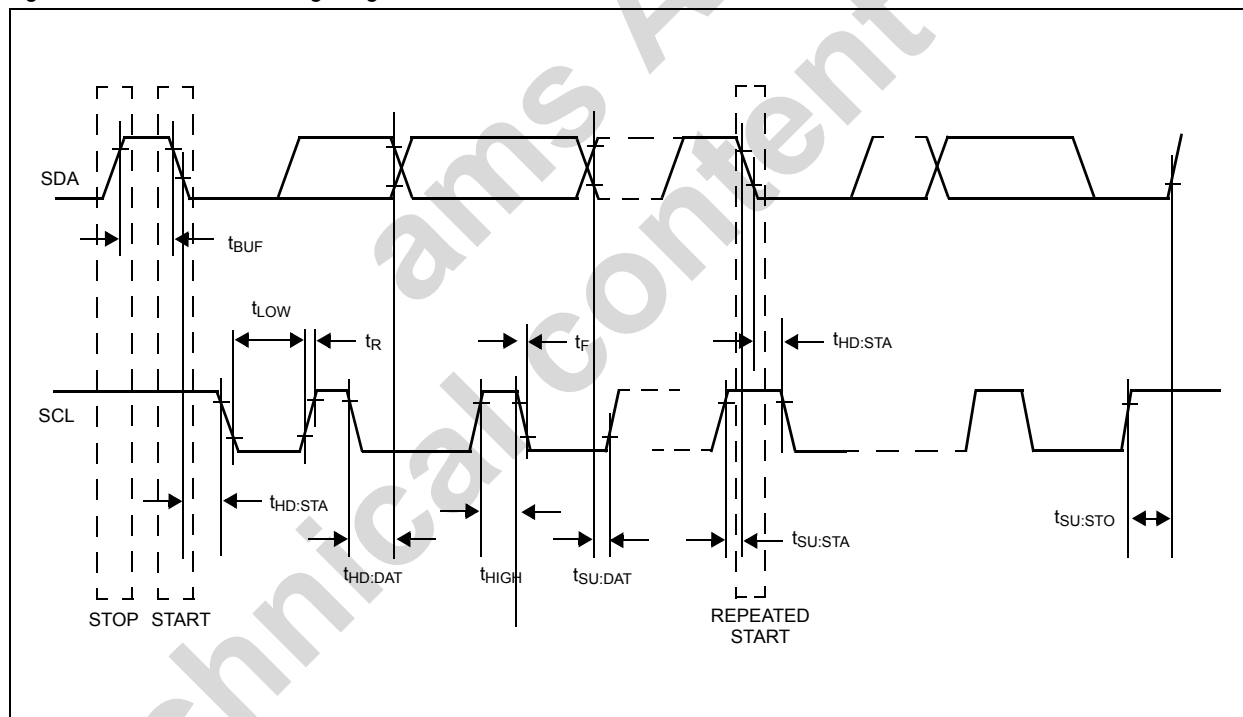
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T _{OVTEMP}	Overtemperature Protection	Junction temperature		144		°C
T _{OVTEMPHYST}	Overtemperature Hysteresis			5		°C
t _{FLASHTIMER}	Flash Timer	Can be adjusted by register <code>flash_timer</code> (see page 16)	-7.5%	30 to 480	+7.5%	ms
V _{UVLO}	Undervoltage Lockout ³	Falling V _{VIN}	2.3	2.4	2.5	V
		Rising V _{VIN}	V _{UVLO} +0.05	V _{UVLO} +0.1	V _{UVLO} +0.15	V
Digital Interface						
V _{IH}	High Level Input Voltage	Pins SCL, SDA ⁴	1.26		V _{VIN} -0.2	V
V _{IL}	Low Level Input Voltage		0.0		0.54	V
V _{OL}	Low Level Output Voltage	Pin SDA with pullup >1kΩ to digital supply <2V, V _{VIN} >2.7V			0.3	V
I²C interface timings - see Figure 3 on page 6						
t _{WAKEUP}	Wakeup Time	Minimum time from SDA or SCL going high to first I ² C start command	500			μs
t _{TIMEOUT}	I ² C timeout time	In flash, assist light and indicator mode if SCL and SDA are L for t _{TIMEOUT} , the AS3644 enters automatically shutdown mode		35		ms
f _{SCLK}	SCL Clock Frequency		1/t _{TIMEOUT}		400	kHz
t _{BUF}	Bus Free Time Between a STOP and START Condition		1.3			μs
t _{HD:STA}	Hold Time (Repeated) START Condition ⁵		0.6			μs
t _{LOW}	LOW Period of SCL Clock		1.3			μs
t _{HIGH}	HIGH Period of SCL Clock		0.6			μs
t _{SU:STA}	Setup Time for a Repeated START Condition		0.6			μs
t _{HD:DAT}	Data Hold Time ⁶		0		0.9	μs
t _{SU:DAT}	Data Setup Time ⁷		100			ns
t _R	Rise Time of Both SDA and SCL Signals		20 + 0.1C _B		300	ns
t _F	Fall Time of Both SDA and SCL Signals		20 + 0.1C _B		300	ns
t _{SU:STO}	Setup Time for STOP Condition		0.6			μs
C _B	Capacitive Load for Each Bus Line	C _B — total capacitance of one bus line in pF			400	pF

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

- Limited to max. 5V due to overvoltage protection circuit on pin VOUT
- Due to slope compensation of the current limit, I_{LIMIT} changes with duty cycle - see [Figure 16 on page 9](#).
- Due to the architecture (the supply of the AS3644 is connected to the output VOUT), the undervoltage lockout is only detected when the DCDC converter is not switching
- The logic input levels V_{IH} and V_{IL} allow for 1.8V supplied driving circuit (70%/30% of 1.8V)
- After this period, the first clock pulse is generated.
- A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} =$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{Rmax} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.

Timing Diagrams

Figure 3. I²C interface Timing Diagram

7 Typical Operating Characteristics

$V_{IN} = 3.7V$, $T_A = +25^{\circ}C$ (unless otherwise specified)

Figure 4. DCDC Efficiency vs. V_{IN}

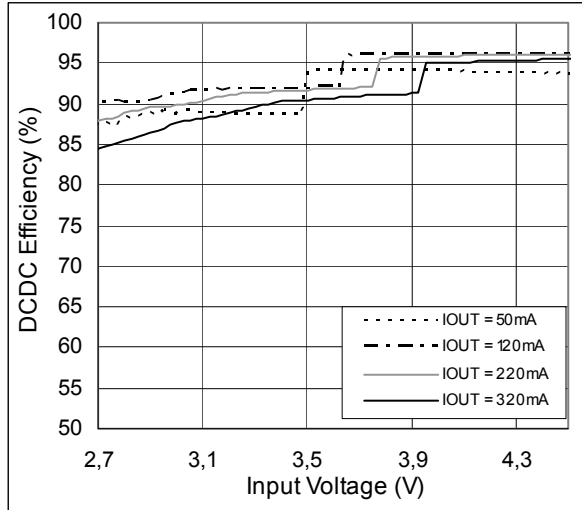


Figure 5. Application Efficiency (P_{LED}/P_{VIN}) vs. V_{IN}

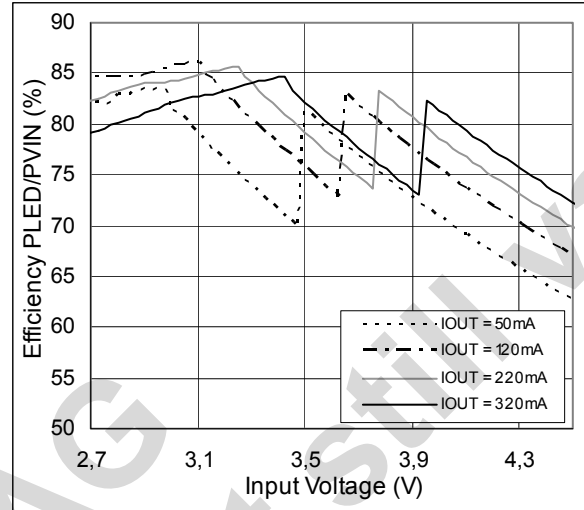


Figure 6. ILED Startup ($I_{LED_OUT}=300mA$)

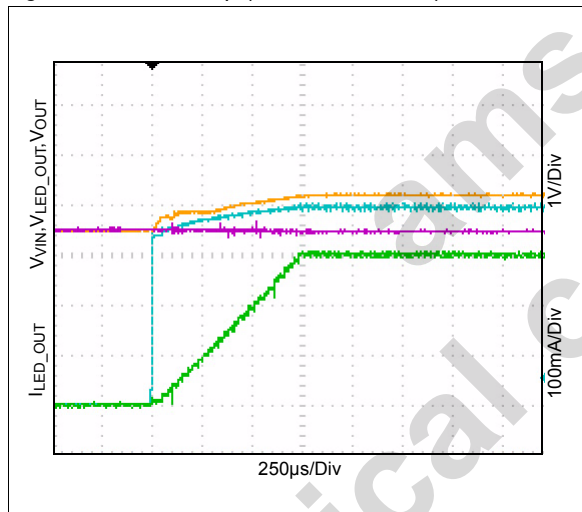


Figure 7. I_{VIN} Startup ($I_{LED_OUT}=300mA$)

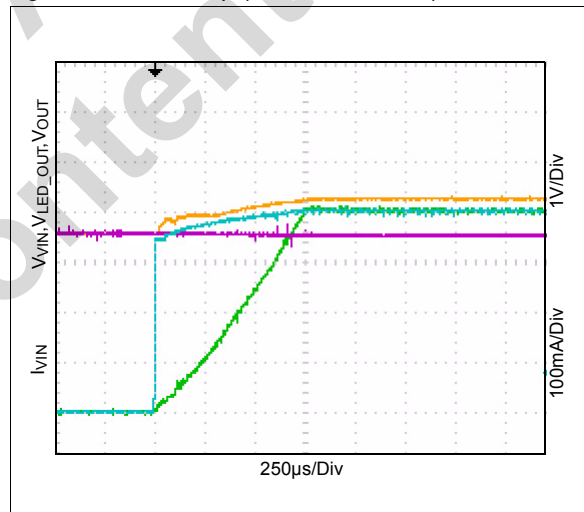


Figure 8. ILED Startup ($I_{LED_OUT}=51.6mA$)

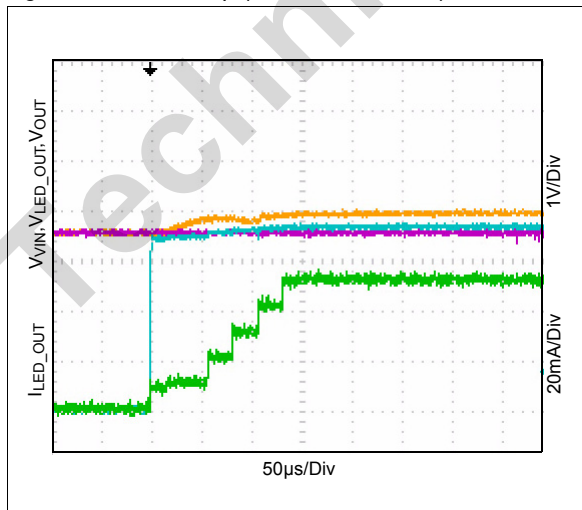


Figure 9. V_{OUT} / I_{LED_OUT} ripple, $I_{LED_OUT} = 300mA$

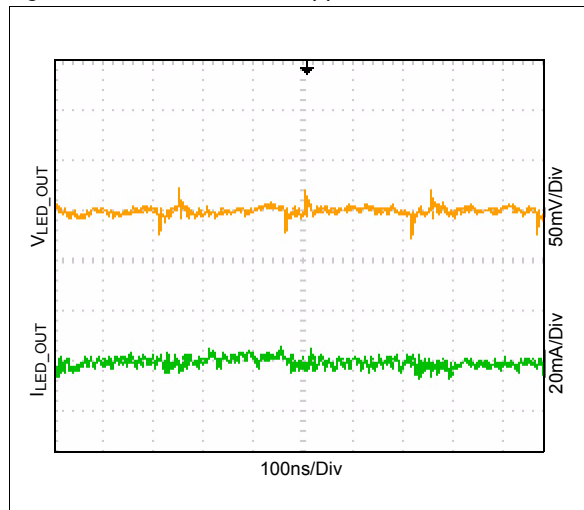


Figure 10. ILED Rampdown (ILED_OUT=300mA)

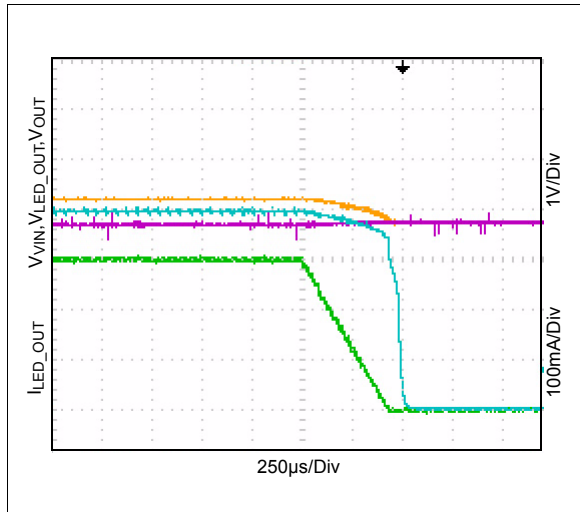


Figure 11. ILED_OUT Linearity of current sink

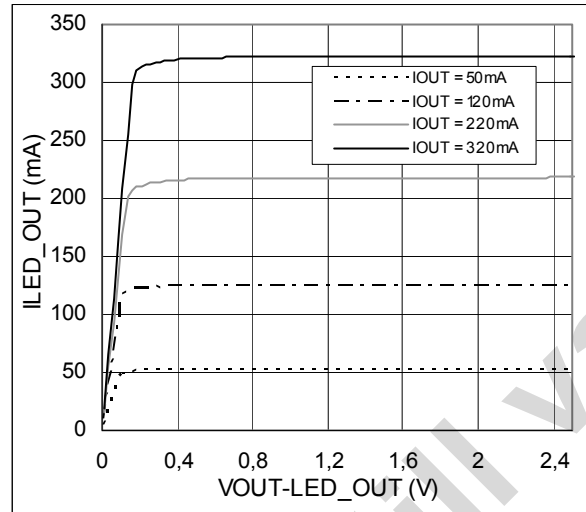


Figure 12. ILED_OUT vs. TAMB

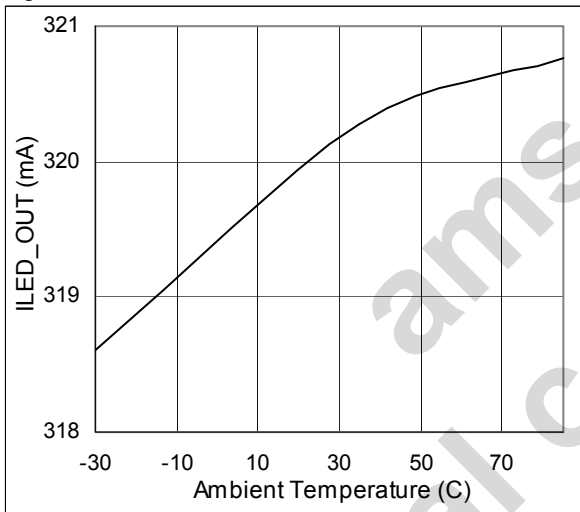


Figure 13. Oscillator frequency fCLK vs. TAMB

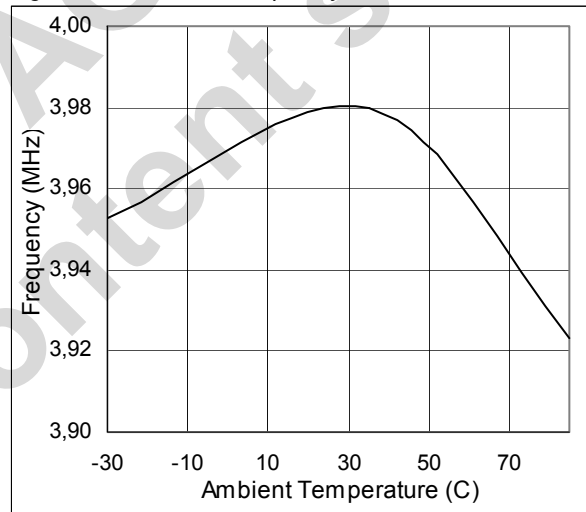


Figure 14. DCDC fCLK change 4MHz->1MHz(300mA)

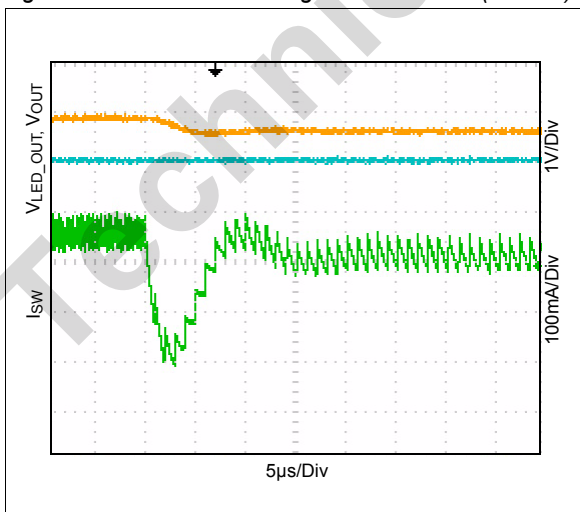
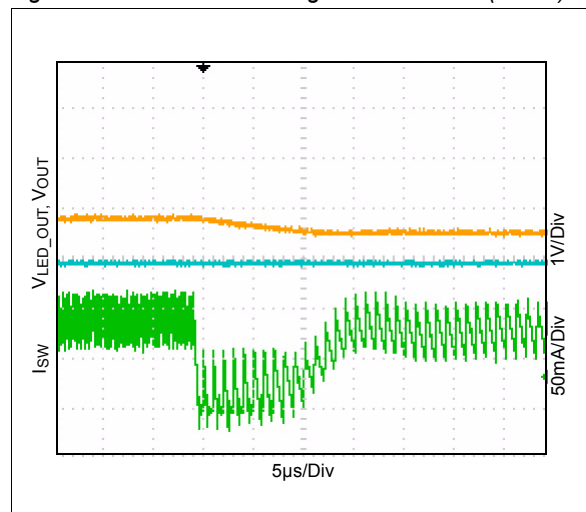


Figure 15. DCDC fCLK change 4MHz->1MHz(51mA)



8 Detailed Description

The AS3644 is a high performance DCDC step up converter with internal PMOS and NMOS switches. The switching frequency of 4MHz allows the use of tiny coils. Its output is connected to a flash LED by an internal current source.

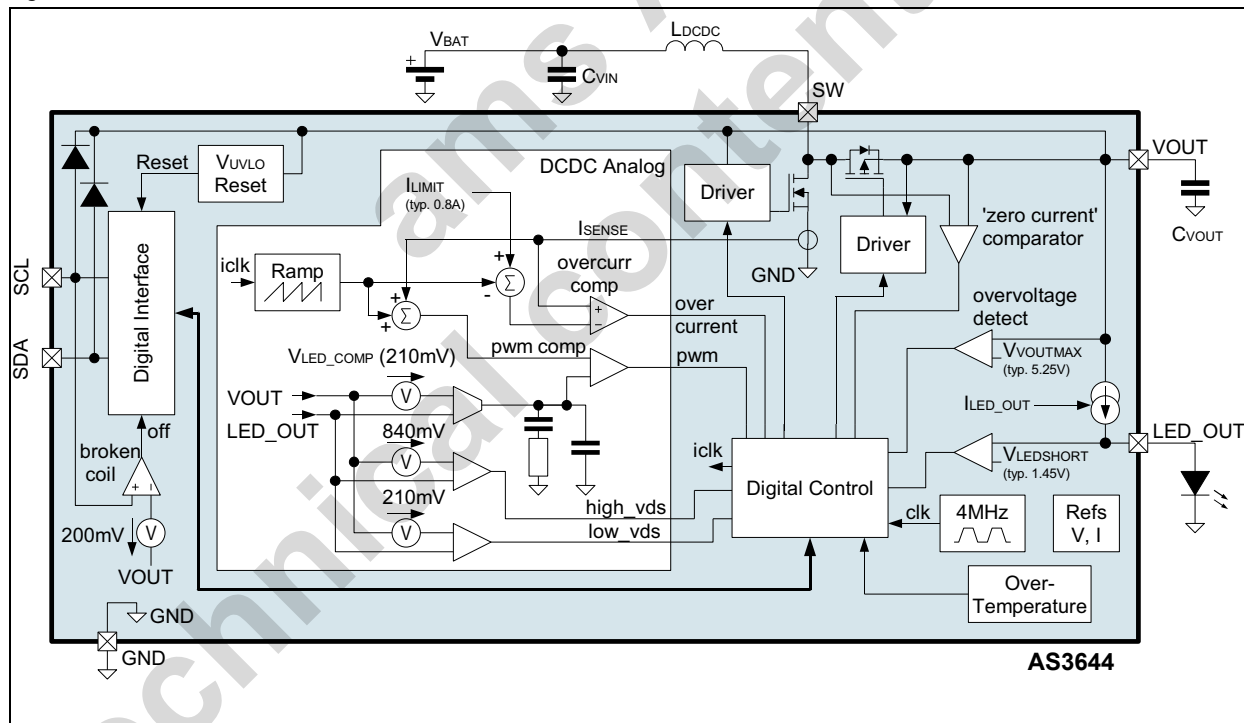
The AS3644 is controlled by an I²C interface. All timings and currents can be accurately adjusted by this interface. It support following operating modes:

1. Flash mode (enabled by `mode=11`):
The LED current (260mA...320mA) is defined by register `flash_current`. A timer defines the output flash duration (30ms...480ms in 30ms steps defined by register `flash_timer`). The flash is started immediately after the end of the I²C command.
If SCL and SDA are L for more than `tTIMEOUT`, shutdown mode is automatically entered.
2. Assist light mode (=video or torch light mode) (enabled by `mode=10`):
The LED current (51.6mA or 72.3mA) is defined by register `assist_current`. The current is enabled until another mode is chosen by the interface.
If SCL and SDA are L for more than `tTIMEOUT`, shutdown mode is automatically entered.
3. Shutdown mode (`mode=00`), `SCL=0V`, `SDA=0V`:
The DCDC and the current source is disabled and the AS3644 is configured to draw minimum current.

Internal Circuit

The AS3644 includes a fixed frequency DCDC step-up with accurate startup control. Together with the output current source (on LED_OUT) it includes protection and safety functions as shown in the following internal blockdiagram:

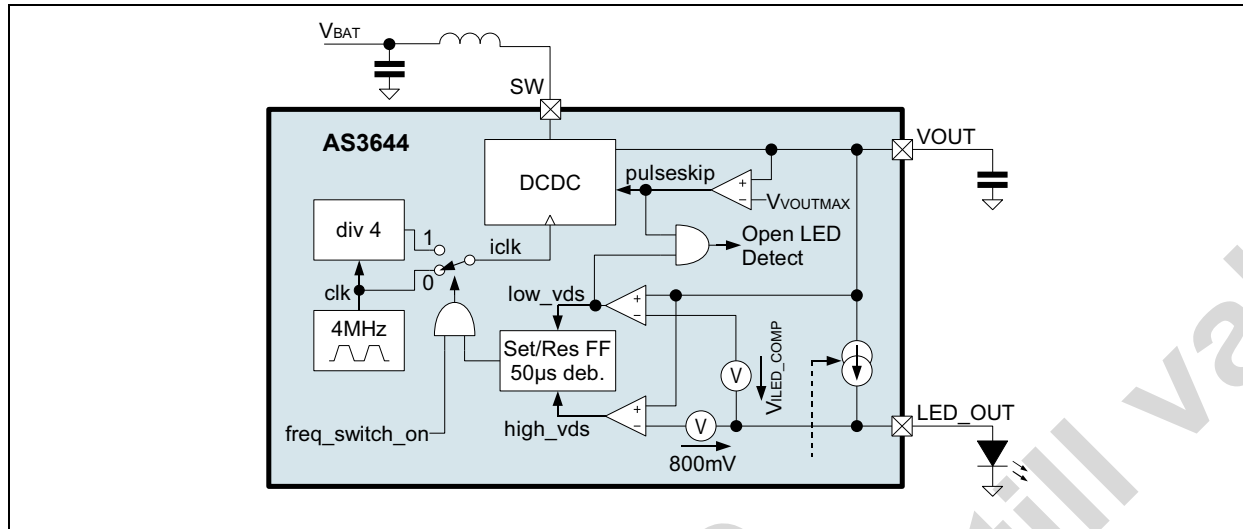
Figure 16. AS3644 internal circuit



The DCDC converter always operates in PWM mode (exception: PFM mode is allowed during startup) to reduce EMI in EMI sensitive systems. For flash and assist light mode and high duty cycles close to 100% on-time (maximum duty cycle) of the PMOS, the DCDC converter can switch into a 1MHz operating mode and maximum duty cycle to improve efficiency for this load condition. The DCDC converter returns back to its normal 4MHz operating frequency when load or supply conditions change. Due to this switching between two fixed frequencies the noise spectrum of the system is exactly defined and predictable. If improved efficiency is required, the fixed switching between 1MHz / 4MHz can be disabled by `freq_switch_on` (see page 15)=0. In this case pulsed skip will be used.

The internal circuit for switching between these two frequencies is shown in Figure 17:

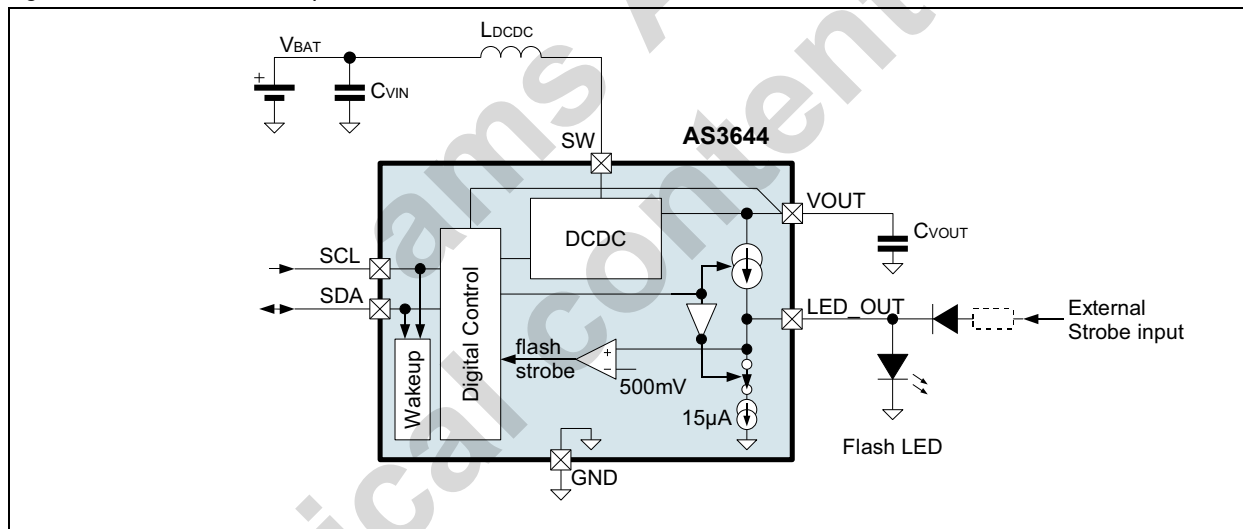
Figure 17. Internal circuit of 4MHz/1Mhz selection



External Strobe Input

To start the flash operation by an hardware input using an external strobe input, use schematic shown in [Figure 18](#):

Figure 18. External strobe input



To enable this function, program the flash timer with the exact flash duration (by programming [flash_timer](#)) and set [external_strobe](#)=1. The AS3644 waits for an external strobe signal on pin LED_OUT and starts the flash pulse with a duration defined by [flash_timer](#).

Protection and Fault Detection Functions

The protection functions protect the AS3644 and the LED(s) against physical damage. In most cases a register bit is set, which can be readout with the interface. The fault bits are cleared¹ by a readout of the fault register.

1. Except overtemperature protection bit [fault_overtemp](#): This bit can be cleared once the temperature drops below $T_{OVTEMP} - T_{OVTEMPHYST}$.

DCDC Overvoltage Protection

In case of no or a broken LED at the pin LED_OUT and an enabled DCDC converter, the voltage on VOUT rises until it reaches $V_{VOUTMAX}$ (overvoltage condition) and the voltage across the current source does not reach regulation ($V_{OUT}-V_{LED} < V_{ILED_COMP}$). If this condition is detected, the DCDC converter is stopped, the current sources are disabled and the bit `fault_ovp` (see page 17) is set.

DCDC Broken Coil Detection

If the coil LDCDC is broken, the AS3644 is not powered by the pin SW connected to VOUT by the internal switch. Due to the protection diodes between SCL to VOUT and SDA to VOUT, the AS3644 can be powered through these diodes. The AS3644 detects this error condition by comparing the voltage on SCL and VOUT. If the voltage on VOUT is lower compared to the voltage on SCL, the AS3644 will ignore any I²C write commands. Therefore the application can simply detect this condition.

Note: Due to the broken coil detection, the high levels of SDA and SCL should be always below the supply voltage.

LED Short Circuit Protection

After the startup of the DCDC converter, the voltage on LED_OUT is continuously monitored and compared against V_{LED_SHORT} . If the voltage stays below V_{LED_SHORT} , the DCDC is stopped (as a shorted LED is assumed), the current sources are disabled and the bit `fault_led_short` (see page 17) is set.

Overtemperature Protection

The junction temperature of the AS3644 is continuously monitored. If the temperature exceeds T_{OVTEMP} , the DCDC is stopped, the current sources are disabled and the bit `fault_overtemp` (see page 17) is set. The driver cannot be re-enabled unless the junction temperature drops below $T_{OVTEMP}-T_{OVTEMPHYST}$.

Flash Timer

The duration of the flash is defined by the register `flash_timer` (see page 16). After the timer expires, the DCDC is stopped and the flash current source (on pin LED_OUT) is disabled.

Supply undervoltage Protection

If the voltage on the pin VOUT (=battery voltage) is or falls below V_{UVLO} , the AS3644 is kept in shutdown state and in all registers are set to their default state.

Note: During operation of the DCDC converter, the supply undervoltage protection will still monitor the DCDC output voltage only. Therefore the supply undervoltage protection will only monitor the battery voltage if the DCDC converter is switched off and the output capacitor is discharged down to the supply voltage.

Wakeup Circuit - Power off detection

In flash, assist light and indicator mode, if SCL and SDA are L for more than $t_{TIMEOUT}$, shutdown mode is automatically entered. This feature automatically detects a power-off of the controlling circuit driving SCL and SDA.

I²C Serial Data Bus

The AS3644 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The AS3644 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The AS3644 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 19):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

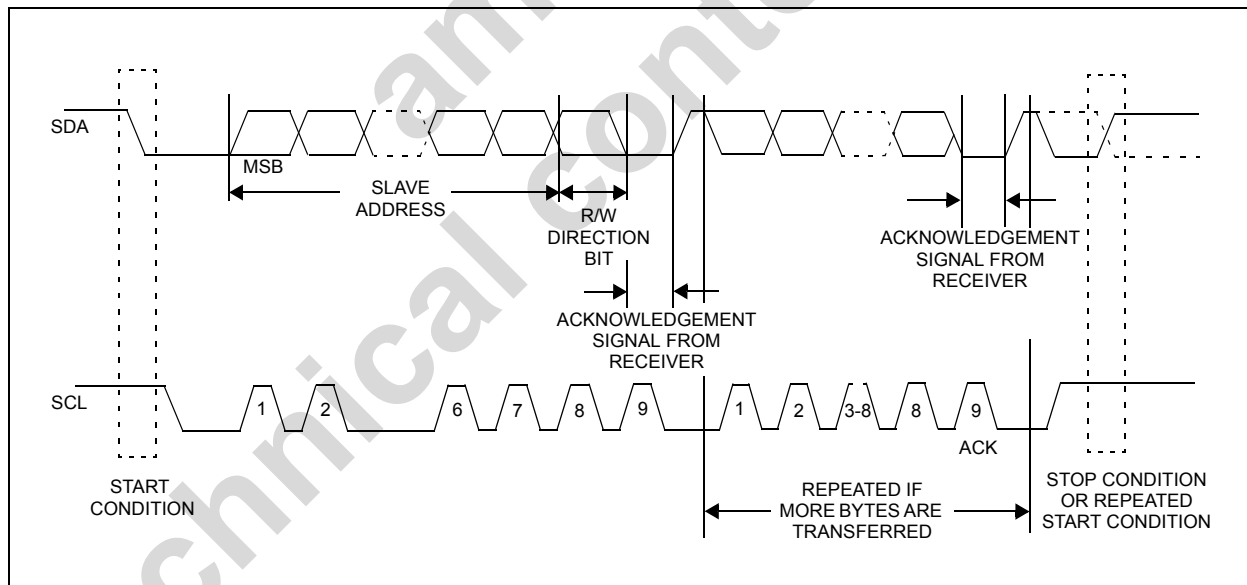
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 19. Data Transfer on I²C Serial Bus



Depending upon the state of the R/W bit, two types of data transfer are possible:

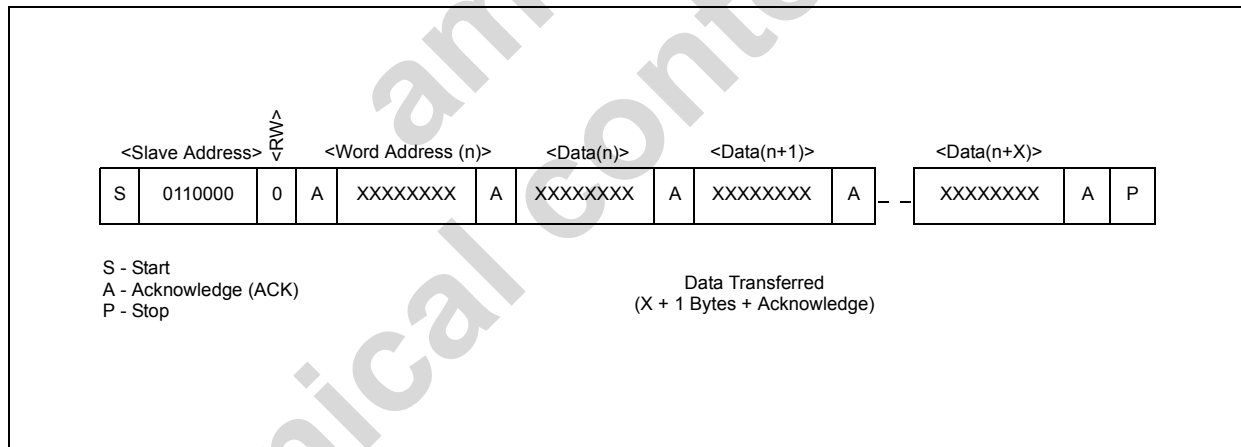
1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses

and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS3644 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 20). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AS3644 address, which is 0110000, followed by the direction bit (R/W), which, for a write, is 0.² After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the AS3644 acknowledges the slave address + write bit, the master transmits a register address to the AS3644. This sets the register pointer on the AS3644. The master may then transmit zero or more bytes of data, with the AS3644 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.
2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS3644 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 21 and Figure 22). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS3644 address, which is 0110000, followed by the direction bit (R/W), which, for a read, is 1.³ After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS3644 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS3644 must receive a “not acknowledge” to end a read.

Figure 20. Data Write - Slave Receiver Mode



2. The address for writing to the AS3644 is 60h = 01100000b

3. The address for read mode from the AS3644 is 61h = 01100001b

Figure 21. Data Read (from Current Pointer Location) - Slave Transmitter Mode

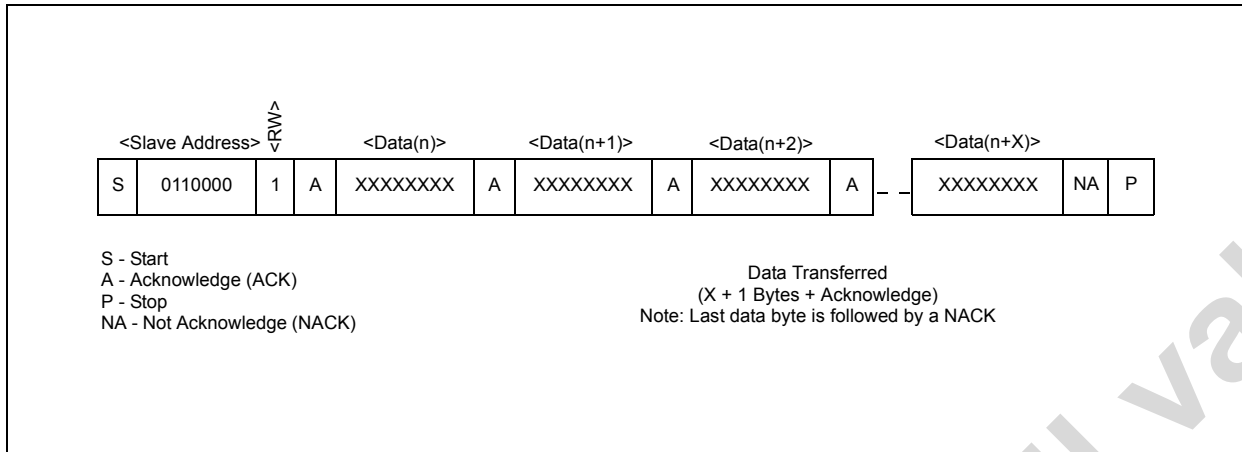
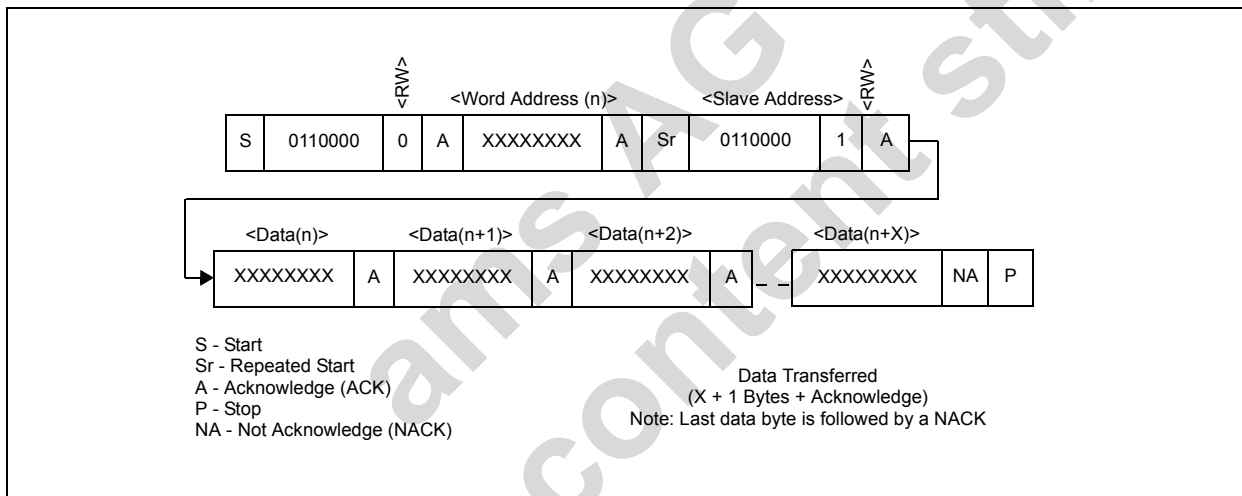


Figure 22. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



Register Description

Table 4. *Design Info Register*

Addr: 0		Design Info Register		
This register has a fixed ID				
Bit	Bit Name	Default	Access	Description
7:0	fixed_id	13h	R	This is a fixed identification (e.g. to verify the I ² C communication)

Table 5. *Version Control Register*

Addr: 1		Version Control Register		
This register defines design versions				
Bit	Bit Name	Default	Access	Description
3:0	version	Xh	R	AS3644 version number
7:4	reserved	Xh	R	reserved - don't use

Table 6. *Current Set Register*

Addr: 2		Current Set Register			
This register defines the Current Settings					
Bit	Bit Name	Default	Access	Description	
1:0	reserved	0h	R	reserved - don't use	
2	freq_switch_on	1	R/W	0	Exact frequency switching between 4MHz/1MHz for assist and flash modes for operation close to maximum pulsewidth - see Figure 17 on page 10
				1	Pulseskip operation is allowed for all modes - results in better efficiency
4:3	reserved	10	R	reserved - don't use	
5	assist_current	1	R/W	Define the current on pin LED_OUT in assist light mode	
				0	I _{LED_OUT} = 51.6mA
				1	I _{LED_OUT} = 72.3mA
7:6	flash_current	10	R/W	Define the current on pin LED_OUT in flash mode	
				00	I _{LED_OUT} = 260mA
				01	I _{LED_OUT} = 280mA
				10	I _{LED_OUT} = 300mA
				11	I _{LED_OUT} = 320mA

Table 7. Control Register

Addr: 3		Control Register			
		This register defines the operating mode and different protection functions in I ² C interface			
Bit	Bit Name	Default	Access	Description	
3:0	flash_timer	4h	R/W	Define the duration of the flash timer	
				0h	30ms
				1h	60ms
				2h	90ms
				3h	120ms
				4h	150ms default value
				5h	180ms
				6h	210ms
				7h	240ms
				8h	270ms
				9h	300ms
				Ah	330ms
				Bh	360ms
				Ch	390ms
				Dh	420ms
				Eh	450ms
Fh	480ms				
5:4	mode	00	R/W	AS3644 operating mode selection	
				00	Shutdown mode
				01	Shutdown mode, readout of this register will return 00b
				10	Assist light mode ¹ with assist_current
11	Flash mode with duration flash_timer with flash_current				
6	reserved	0	R	reserved - don't use	
7	external_strobe ²	0	R/W	External strobe signal from pin LED_OUT	
				0	no external strobe
				<p>A flash pulse with current defined by flash_current is triggered on a rising edge on LED_OUT (e.g. due to an external signal pulling it high). At the same time this register is automatically cleared. After the flash pulse (duration defined by flash_timer) the AS3644 returns to shutdown mode.</p> <p>Note: Setting this bit automatically sets mode (see page 16)=11 (flash mode)</p> <p>A ongoing flash started with external_strobe can be stopped by writing '0' to external_strobe and '00' to mode.</p>	

1. Torch mode and assist light mode share the same operating mode and identical currents.
2. Before changing `external_strobe` register, contact austriamicrosystems to obtain the unlock sequence for this register (needs one additional register write access for enabling access to this register).

Table 8. *Fault Register*

Addr: 4		Fault Register			
This register identifies all the different fault conditions and provide information about the LED detection					
Bit	Bit Name	Default	Access	Description	
4:0	reserved	0	R	reserved - don't use	
5	fault_overtemp	0	R	see Overtemperature Protection on page 11	
				0	No fault
				1	Junction temperature limit has been exceeded
6	fault_led_short	0	R	see LED Short Circuit Protection on page 11	
				0	No fault
				1	A shorted LED is detected (pin LED_OUT)
7	fault_ovp	0	R	see DCDC Overvoltage Protection on page 11	
				0	No fault
				1	An overvoltage condition is detected (pin VOUT)

Register Map

Table 9. *Register Map*

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Design Info	0	13h	fixed_id							
Version Control	1	XXh	reserved				version			
Current Set	2	B4h	flash_current	assist_current	reserved	reserved	freq_switch_on	reserved	reserved	reserved
Control	3	04h	external_strobe	reserved	mode	reserved	reserved	flash_timer	reserved	reserved
Fault	4	00h	fault_ovp	fault_led_short	fault_overtemp	reserved	reserved	reserved	reserved	reserved

9 Application Information

The AS3644 can be directly connected to an (existing) I²C bus (e.g. from the baseband or camera processor). All functions are accessible by this interface.

External Components

Input Capacitor C_{VIN}

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are required for input decoupling and should be located as close to the device as is practical.

Table 10. Recommended Input Capacitor

Part Number	C	TC Code	ESR	Rated Voltage	Size	Manufacturer
CL05A395MQ5NQKL	4.7μF +/-10% >1.6μF @ V _{VIN}	X5R	<20mΩ	6V3	0402	Samsung Electro-Mechanics www.sem.samsung.co.kr

If a different input capacitor is chosen, ensure similar ESR value and at least 1.6μF capacitance at the maximum input supply voltage. Larger capacitor values (C) may be used without limitations.

Output Capacitor C_{VOUT}

Low ESR capacitors should be used to minimize V_{OUT} ripple. Multi-layer ceramic capacitors are recommended since they have extremely low ESR and are available in small footprints. The capacitor should be located as close to the device as is practical.

X5R dielectric material is recommended due to their ability to maintain capacitance over wide voltage and temperature range.

Table 11. Recommended Output Capacitor

Part Number	C	TC Code	ESR	Rated Voltage	Size	Manufacturer
ECJUNBPJ155K	2x1.5μF +/-15%	X5R	<10mΩ	6V3	0405 2-array	Panasonic www.panasonic.com
CL14A185MQ8SAKL						Samsung Electro-Mechanics www.sem.samsung.co.kr

If a different output capacitor is chosen, ensure similar ESR values and at least 1.0μF capacitance at maximum output voltage.

Inductor L_{DCDC}

The fast switching frequency (4MHz) of the AS3644 allows for the use of small SMDs for the external inductor. The inductor should have low DC resistance (DCR) to reduce the I²R power losses - high DCR values will reduce efficiency.

Table 12. Recommended Inductor

Part Number	L	DCR	L @ 0.9A	Size	Manufacturer
LQM21PN1R0NGC	1.1μH	100mΩ	>0.7μH	2x1.25x0.9mm	Murata www.murata.com
ELGTEA1R0SN	1.0μH		>0.7μH	2x1.25x0.9mm	Panasonic www.panasonic.com
CIG21K1R0SCE	1.17μH	135mΩ	>0.7μH	2x1.25x0.9mm	Samsung Electro-Mechanics www.sem.samsung.co.kr

Table 12. Recommended Inductor (Continued)

Part Number	L	DCR	L @ 0.9A	Size	Manufacturer
CKP2012N1R0M	1.0 μ H	110m Ω	>0.7 μ H	2x1.25x0.9mm	Taiyo Yuden www.t-yuden.com
MLP2012L1R0MT	1.0 μ H		>0.7 μ H	2x1.25x0.9mm	TDK www.tdk.com
MDT2012-CR1R0AN	1.0 μ H	110m Ω	>0.7 μ H	2x1.25x0.9mm	Toko www.toko.co.jp

If a different inductor is chosen, ensure similar DCR values and at least 0.7 μ H inductance at 0.9A input current.

LED

Use LED and optics as required by the system.

Table 13. Recommended LEDs

Part Number	Name	Lumen @ 300mA	Size	Manufacturer
CERAMOS LUW C9SM	Ceramos	55	2.04x1.64x0.75mm	Osram Opto Semiconductors www.osram-os.com
LXCL-PWF3	Luxeon PWF3	30	2.04x1.64x0.7mm	Philips Lumileds www.philipslumileds.com

PCB Layout Guideline

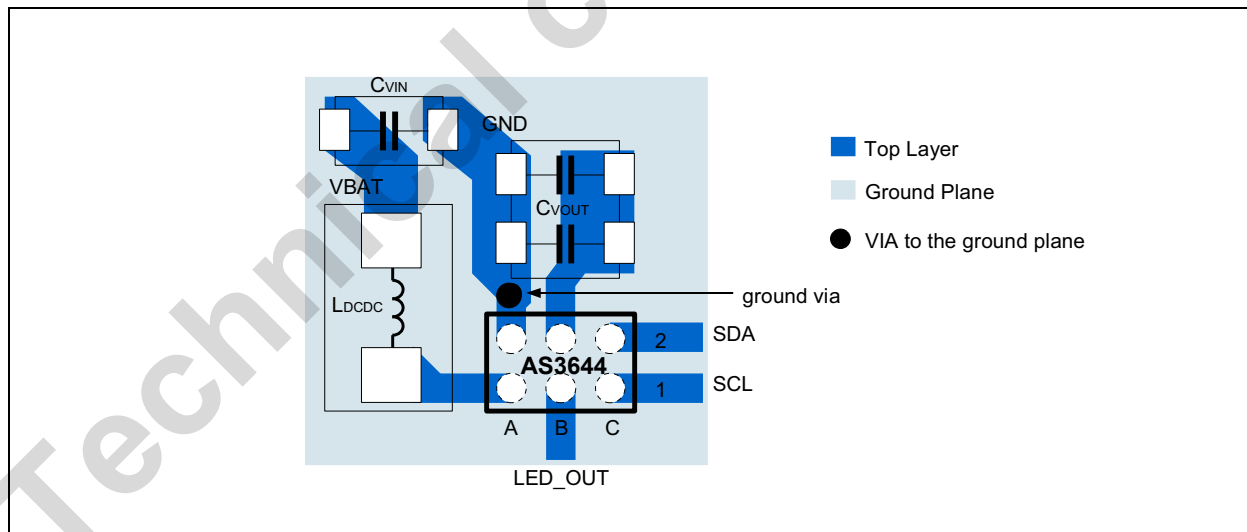
The high speed operation requires proper layout for optimum performance. Route the power traces first and try to minimize the area and wire length of the two high frequency/high current loops:

Loop1: CVIN - LDCDC - pin SW - pin GND - CVIN

Loop2: CVIN - LDCDC - pin SW - pin VOUT - CVOUT - pin GND - CVIN

At the pin GND a single via (or more vias, which are closely combined) connects to the common ground plane. This via(s) will isolate the DCDC high frequency currents from the common ground (as most high frequency current will flow between Loop1 and Loop2 and will not pass the ground plane) - see the 'ground via' in Figure 23.

Figure 23. Layout recommendation



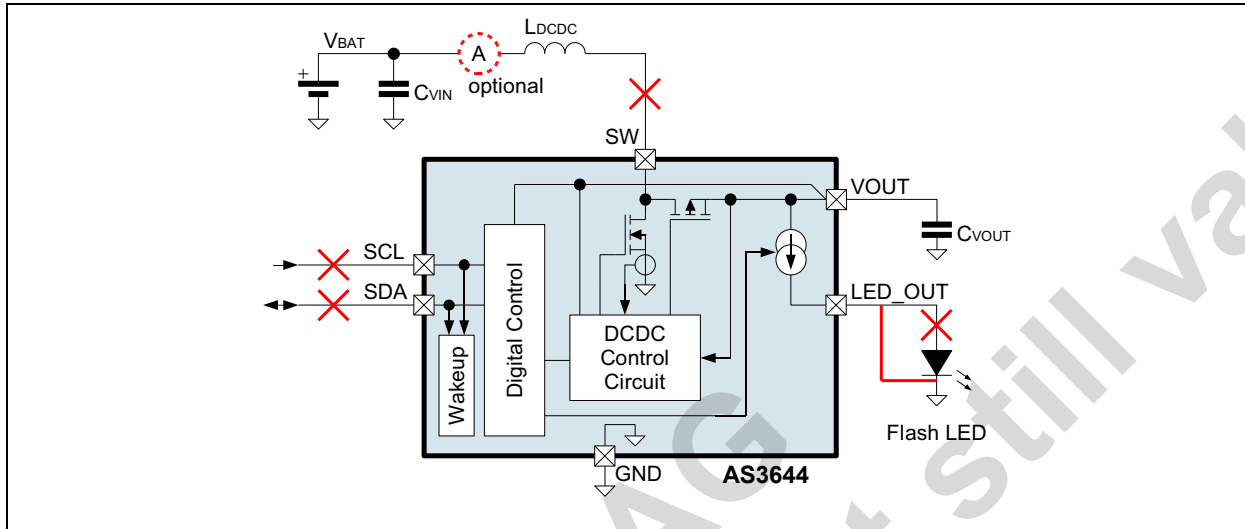
Note: If component placement rules allow, move all components close to the AS3644 to reduce the area and length of Loop1 and Loop2.

The recommended PCB pad size for the AS3644 is 250 μ m.

Application Self Testing Guideline

Using the in-built self testing features of the AS3644, the errors as shown in Figure 24 during the assembling and soldering of the AS3644, can be detected - this simplifies and can reduce cost during manufacturing:

Figure 24. Self Testing - Detecting Assembling and Soldering Errors



The self testing procedure is simple:

1. Write 0x20 into register 0x03 ([Control register](#)) [Enable assist light with default 72mA].
2. Read back⁴ register 0x03 - must return 0x20, otherwise LDCDC or I²C (SCL or SDA) is broken
3. Write 0x00 into register 0x03 [Power off]
4. Read register 0x04 ([Fault register](#)) - must return 0x00, otherwise the LED is open or shorted

See [Table 14](#) to identify the different possible soldering errors:

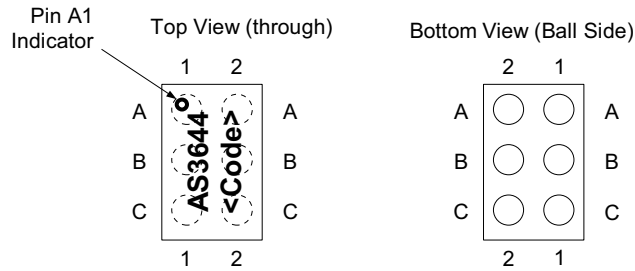
Table 14. How-to identify errors

Error	Identified by
SCL or SDA broken	writing 0x20 to 0x03 and read back of register 0x03 does not return 0x20
LDCDC broken	writing 0x20 to 0x03 and read back of register 0x03 does not return 0x20 - see DCDC Broken Coil Detection on page 11
Flash LED shorted	register <code>fault_led_short</code> (see page 17) is set
Flash LED open	register <code>fault_ovp</code> (see page 17) is set

4. Alternative testing method: Instead of reading the internal registers, the current into the AS3644 can be measured. During assist light mode, the supply current must increase by at least 60mA. If an error is detected, the current source and the DCDC is automatically switched off - see [Protection and Fault Detection Functions on page 10](#)

10 Package Drawings and Markings

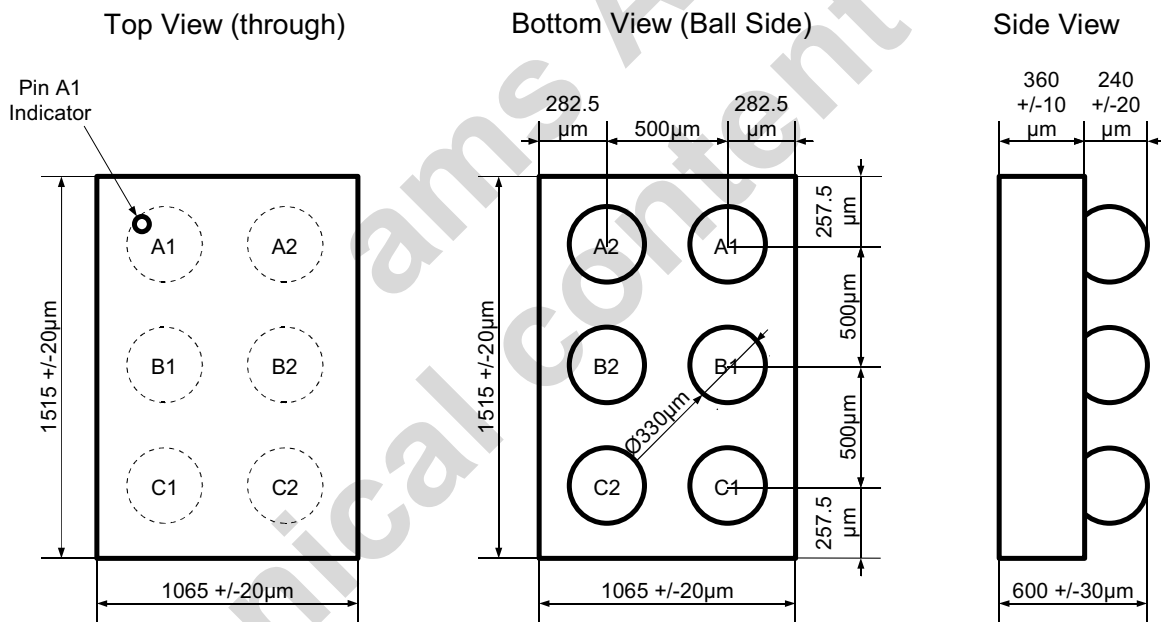
Figure 25. 6pin WL-CSP Marking



Note:

- Line 1: AS3644
- Line 2: <Code>
Encoded Datecode (4 characters)

Figure 26. 6pin WL-CSP Package Dimensions



The coplanarity of the balls is 40 μm.

11 Ordering Information

The devices are available as the standard products shown in [Table 15](#).

Table 15. Ordering Information

Model	Description	Delivery Form	Package
AS3644-ZWLT	Ultra Small Low Cost 320mA Inductive White LED Flash Driver	Tape & Reel	6-pin WL-CSP (1.5mm x 1.1mm x 0.6mm) RoHS compliant / Pb-Free

Note: AS3644-ZWLT

AS3644-

Z Temperature Range: -30°C - 85°C

WL Package: Wafer Level Chip Scale Package (WL-CSP) 1.5x1.1x0.6mm

T Delivery Form: Tape & Reel

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Contact Information

Headquarters

austriamicrosystems AG

Tobelbaderstrasse 30

Schloss Premstaetten

A-8141 Austria

Tel: +43 (0) 3136 500 0

Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

<http://www.austriamicrosystems.com/contact>