# ESD8504G

# ESD Protection Diode

## Low Capacitance Array for High Speed Data Lines

The ESD8504G is designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0/3.1.

### Features

- Low Capacitance (0.5 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- USB 3.0/3.1
- eSATA
- DisplayPort

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating Junction Temperature Range | $T_J$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Lead Solder Temperature − Maximum (10 Seconds) | $T_L$ | 260 | °C |
| IEC 61000−4−2 Contact (ESD)<br>IEC 61000−4−2 Air (ESD) | ESD<br>ESD | ±25<br>±25 | kV<br>kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

**ON Semiconductor®**

www.onsemi.com

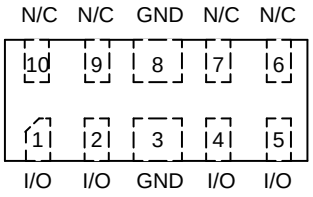
**MARKING DIAGRAM**

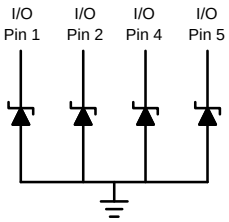
**UDFN10**
**CASE 517BB**


4G = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

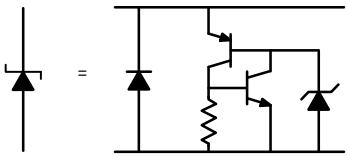
**PIN CONFIGURATION AND SCHEMATIC**




Pins 3, 8

Note: Common GND − Only Minimum of 1 GND connection required



**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| ESD8504GMUTAG | UDFN10 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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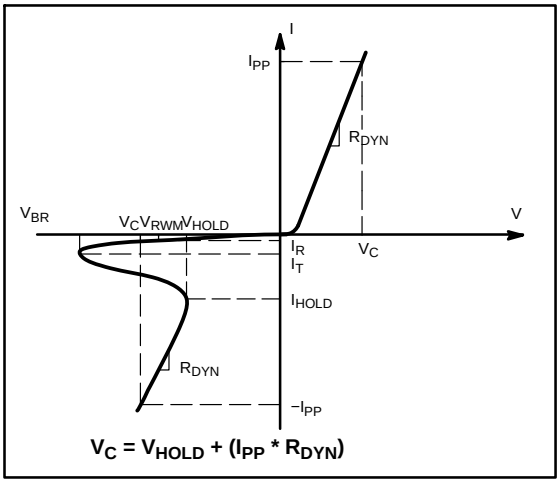
## ELECTRICAL CHARACTERISTICS
($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $V_{RWM}$ | Working Peak Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $V_{HOLD}$ | Holding Reverse Voltage |
| $I_{HOLD}$ | Holding Reverse Current |
| $R_{DYN}$ | Dynamic Resistance |
| $I_{PP}$ | Maximum Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$<br>$V_C = V_{HOLD} + (I_{PP} * R_{DYN})$ |




## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse Working Voltage | $V_{RWM}$ | I/O Pin to GND | | | 3.0 | V |
| Breakdown Voltage | $V_{BR}$ | $I_T$ = 1 mA, I/O Pin to GND | 4.0 | 4.5 | 6.0 | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 3.0 V, I/O Pin to GND | | | 1.0 | μA |
| Holding Reverse Voltage | $V_{HOLD}$ | I/O Pin to GND | | 1.9 | | V |
| Holding Reverse Current | $I_{HOLD}$ | I/O Pin to GND | | 20 | | mA |
| Clamping Voltage (Note 1) | $V_C$ | IEC61000−4−2, ±8 KV Contact | | See Figures 1 and 2 | | V |
| Clamping Voltage TLP (Note 2) See Figures 5 through 8 | $V_C$ | $I_{PP}$ = 8 A<br>$I_{PP}$ = −8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)<br>$I_{PP}$ = 16 A<br>$I_{PP}$ = −16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±15 kV Air) | | 4.75<br>−5.5<br>7.0<br>−8.5 | | V |
| Dynamic Resistance | $R_{DYN}$ | I/O Pin to GND<br>GND to I/O Pin | | 0.3<br>0.4 | | Ω |
| Junction Capacitance (See Figures 9 & 10) | $C_J$ | $V_R$ = 0 V, f = 1 MHz between I/O Pins and GND<br>$V_R$ = 0 V, f = 2.5 GHz between I/O Pins and GND<br>$V_R$ = 0 V, f = 1 MHz, between I/O Pins | | 0.39 | 0.5<br>0.45<br>0.25 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 3 and 4 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 4 ns, averaging window; $t_1$ = 30 ns to $t_2$ = 60 ns.

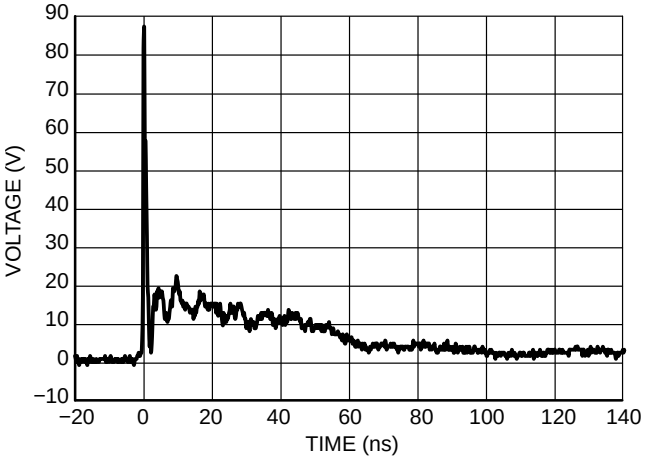



**Figure 1. IEC61000−4−2 +8 kV Contact ESD Clamping Voltage**

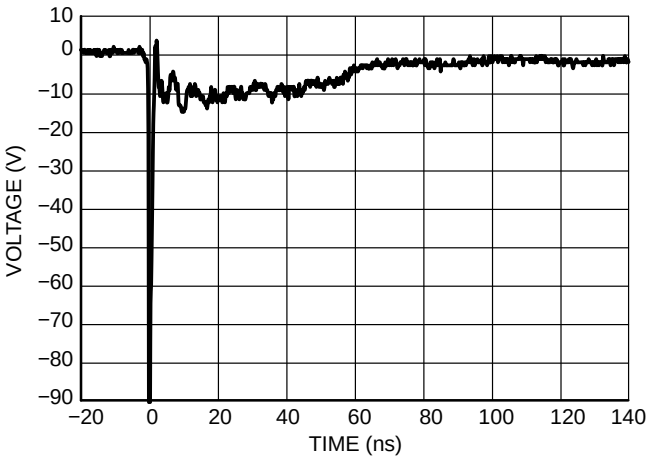



**Figure 2. IEC61000−4−2 −8 kV Contact Clamping Voltage**

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

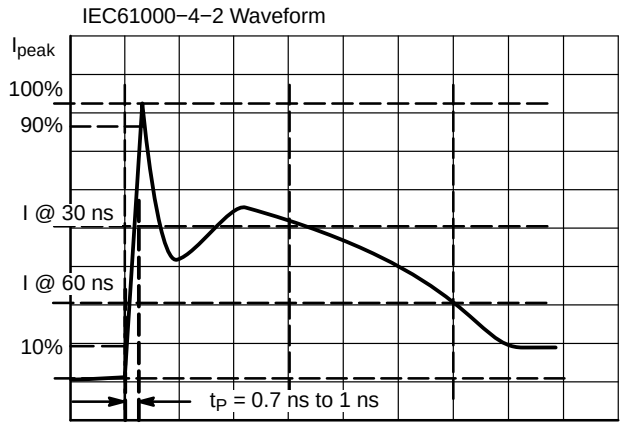



**Figure 3. IEC61000−4−2 Spec**

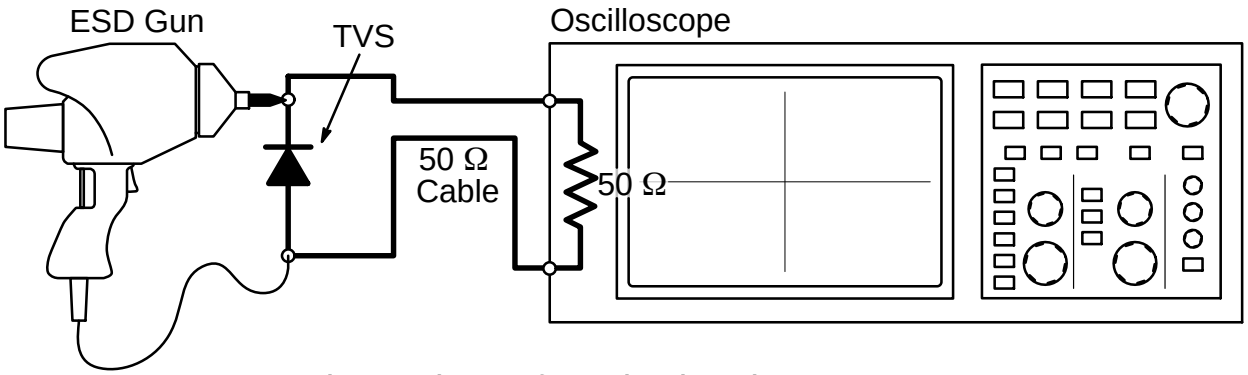



**Figure 4. Diagram of ESD Clamping Voltage Test Setup**

**The following is taken from Application Note AND8307/D − Characterization of ESD Clamping Performance.**

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

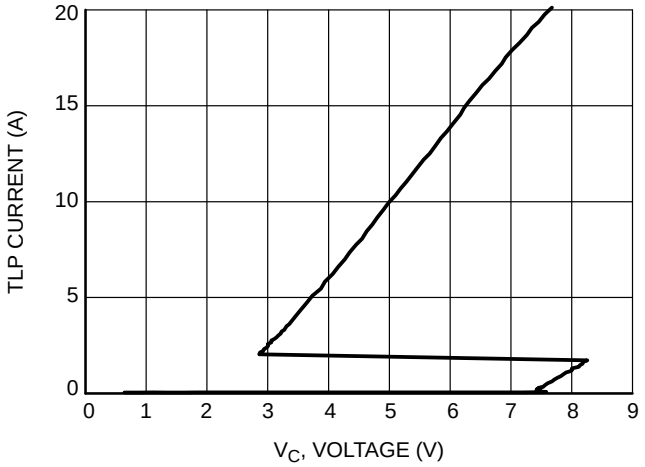



**Figure 5. Positive TLP I−V Curve**

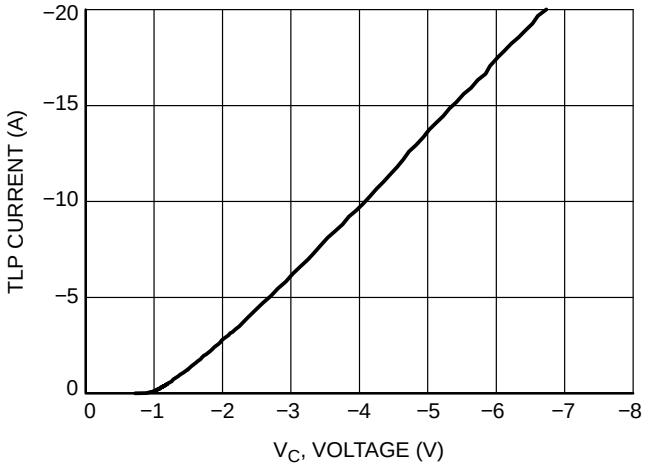



**Figure 6. Negative TLP I−V Curve**

NOTE: TLP parameter: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 300 ps, averaging window: $t_1$ = 30 ns to $t_2$ = 60 ns. $V_{IEC}$ is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

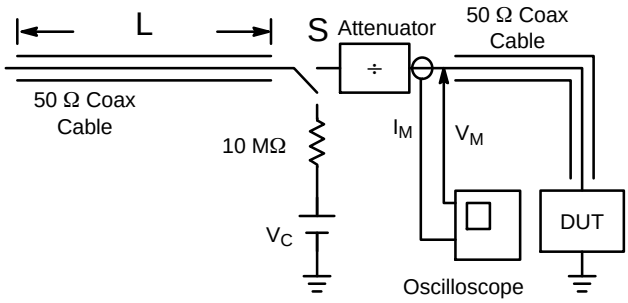



**Figure 7. Simplified Schematic of a Typical TLP System**

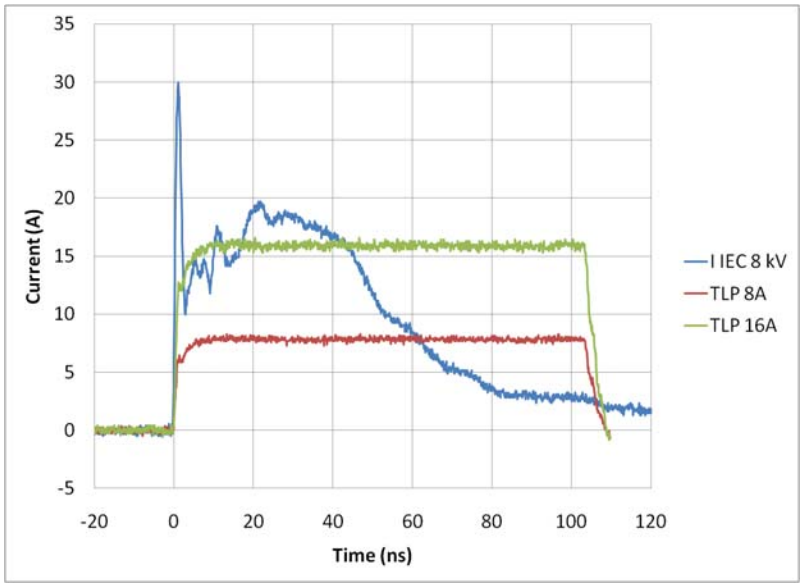



**Figure 8. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms**

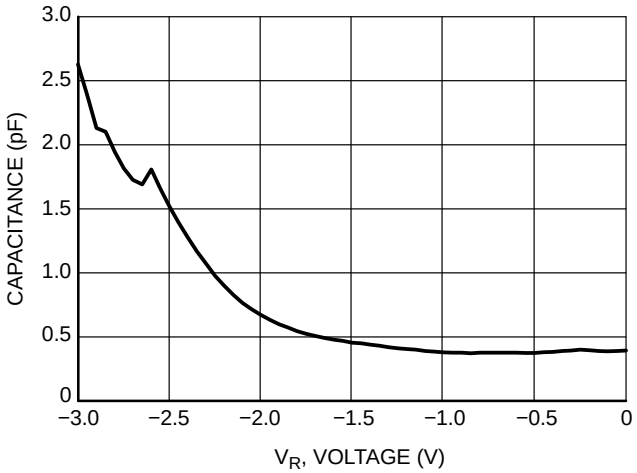



**Figure 9. Junction Capacitance; $V_R$ = −3.0 V − 0 V, f = 1 MHz, I/O − GND, dV/dt = 214 mV/s**

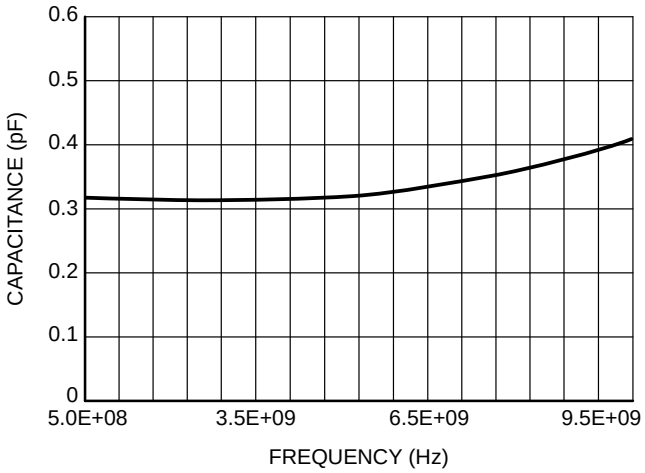
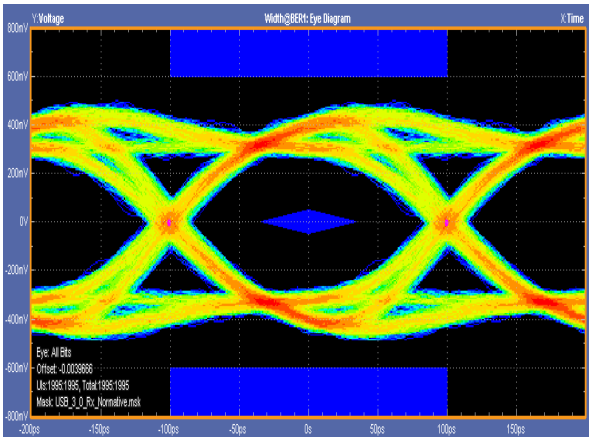



**Figure 10. Junction Capacitance; $V_R$ = 0 V, f = 500 MHz − 10 GHz**



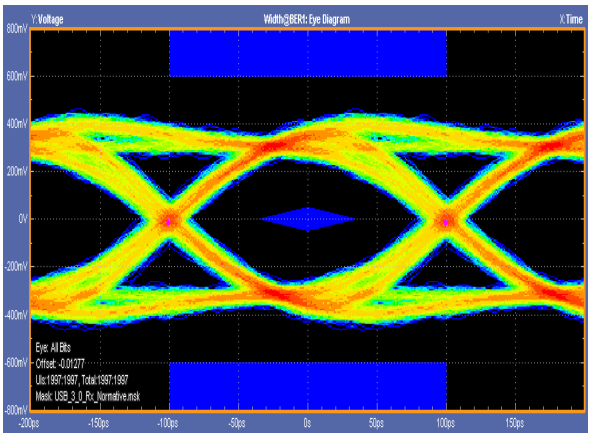




**Figure 11. USB3.0 Eye Diagram with and without ESD8504G. 5 Gb/s**

See application note AND9075/D for further description of eye diagram testing methodology.

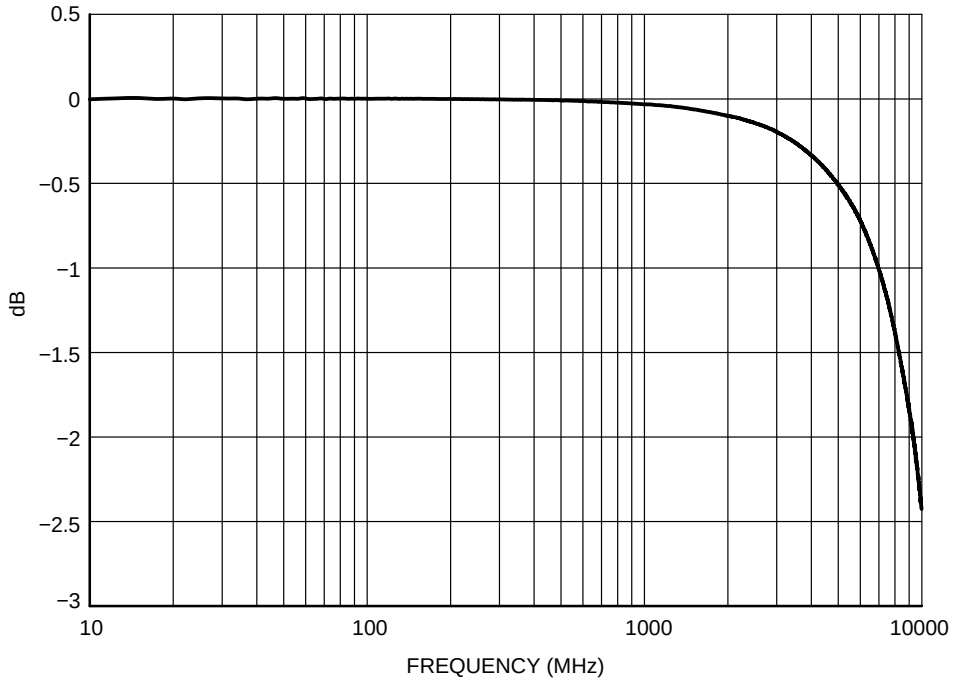



**Figure 12. ESD8504G Insertion Loss**

| Interface | Data Rate (Gb/s) | Fundamental Frequency (GHz) | 3rd Harmonic Frequency (GHz) | ESD8504G Insertion Loss (dB) |
|---|---|---|---|---|
| USB 3.0 | 5 | 2.5 (m1) | 7.5 (m3) | m1 = −0.13<br>m3 = −1.08<br>m2 = −0.48<br>m4 = −10.0 |
| USB 3.1 | 10 | 5.0 (m2) | 15 (m4) | |

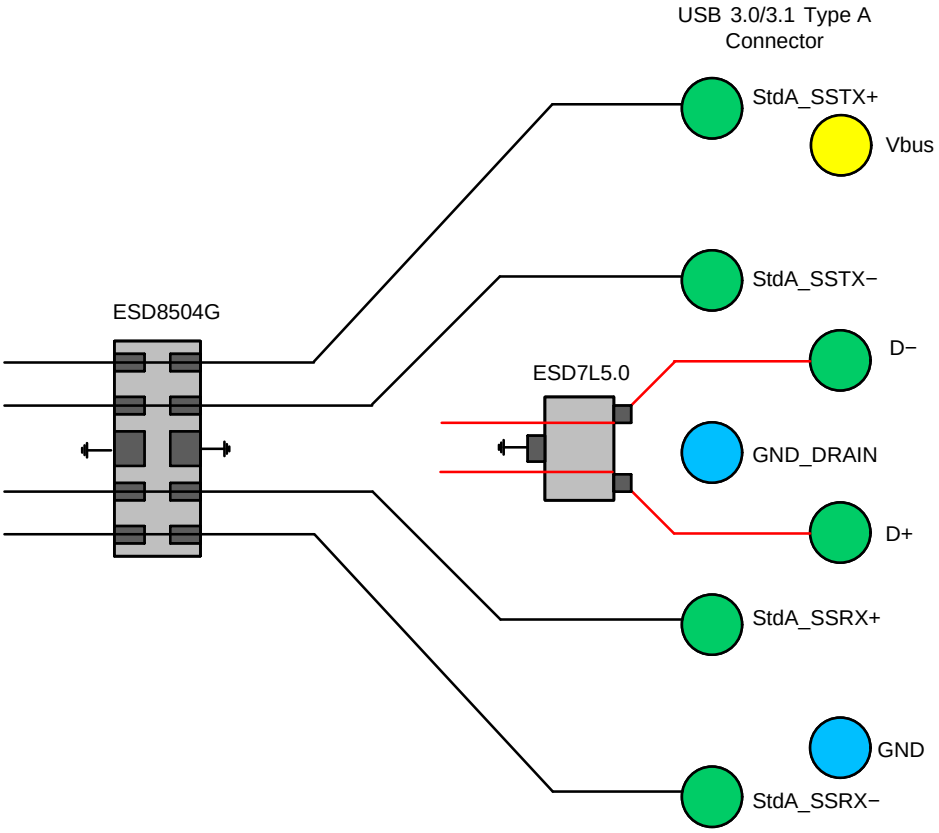



**Figure 13. USB 3.0/3.1 Standard Layout Diagram**

### PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
  - In USB 3.0 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in Figure 14. In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition. For more information on latchup considerations, see below description on Page 8.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
  - Use curved traces when possible to avoid unwanted reflections.
  - Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
  - Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

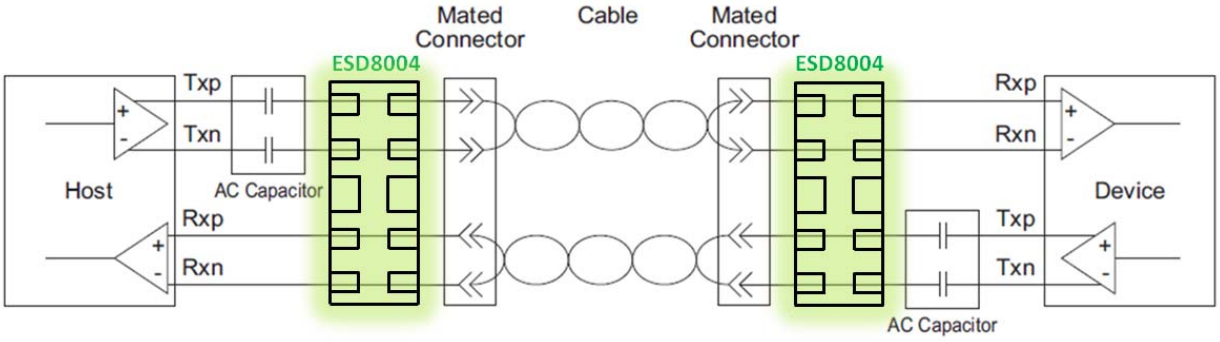
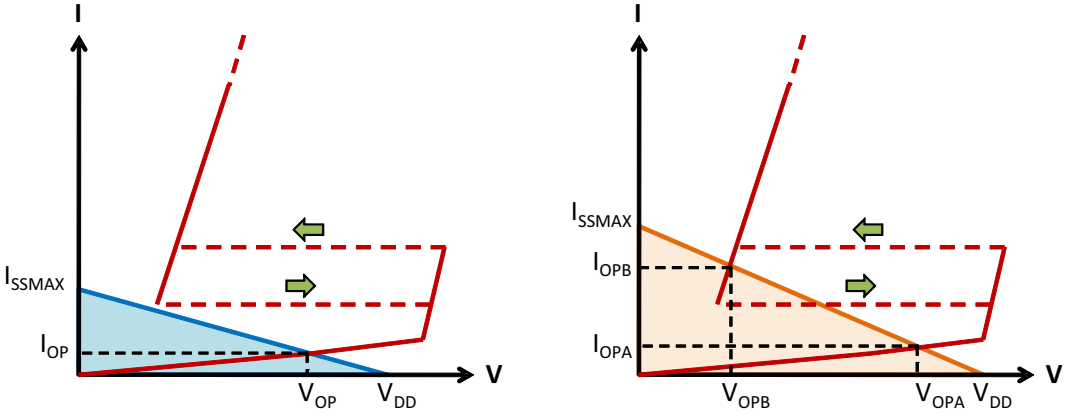



**Figure 14. USB 3.0/3.1 Connection Diagram**

### Latch-Up Considerations

ON Semiconductor's 8000 series of ESD protection devices utilize a snap-back, SCR type structure. By using this technology, the potential for a latch-up condition was taken into account by performing load line analyses of common high speed serial interfaces. Example load lines for latch-up free applications and applications with the potential for latch-up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch-up free load line case, the IV characteristic of the snapback protection device intersects the load-line in one unique point ($V_{OP}$, $I_{OP}$). This is the only stable operating point of the circuit and the system is therefore latch-up free. Please note that for USB 3.0 applications, ESD8504G latch-up free considerations are explained in more detail in the above PCB layout guidelines. In the non-latch up free load line case, the IV characteristic of the snapback protection device intersects the load-line in two points ($V_{OPA}$, $I_{OPA}$) and ($V_{OPB}$, $I_{OPB}$). Therefore in this case, the potential for latch-up exists if the system settles at ($V_{OPB}$, $I_{OPB}$) after a transient. Because of this, ESD8504G should not be used for HDMI applications – ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch-up. Please refer to Application Note AND9116/D for a more in-depth explanation of latch-up considerations using ESD8000 series devices.




ESD8504G Latch−up free:
USB 2.0 LS/FS, USB 2.0 HS, USB 3.0/3.1 SS, DisplayPort

ESD8504G Potential Latch−up:
HDMI 1.4/1.3a TMDS

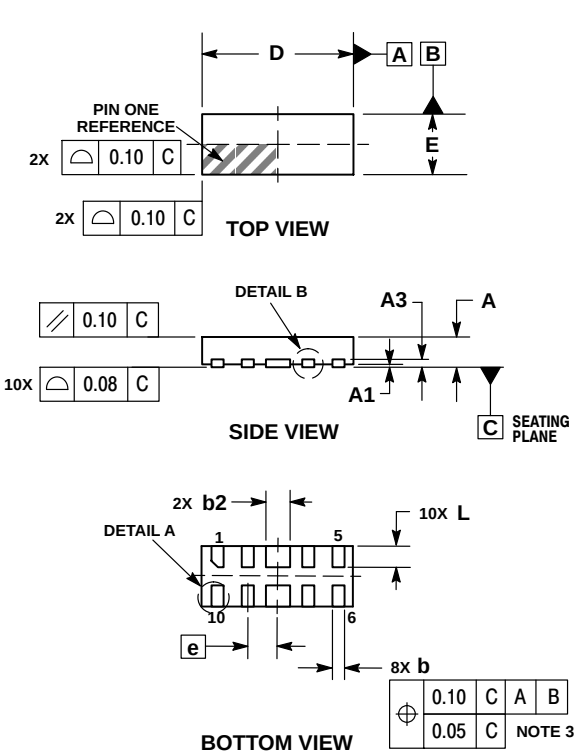
**Figure 15. Example Load Lines for Latch-up Free Applications and Applications with the Potential for Latch-up**

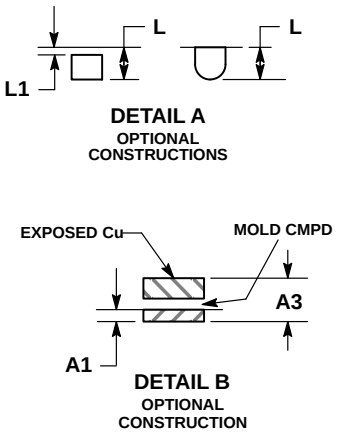
**Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH-UP FREE APPLICATIONS**

| Application | VBR (min) (V) | IH (min) (mA) | VH (min) (V) | ON Semiconductor ESD8000 Series Recommended PN |
|---|---|---|---|---|
| HDMI 1.4/1.3a TMDS | 3.465 | 54.78 | 1.0 | ESD8104, ESD8040 |
| USB 2.0 LS/FS | 3.301 | 1.76 | 1.0 | ESD8504G |
| USB 2.0 HS | 0.482 | N/A | 1.0 | ESD8504G |
| USB 3.0/3.1 SS | 2.800 | N/A | 1.0 | ESD8504G, ESD8006 |
| DisplayPort | 3.600 | 25.00 | 1.0 | ESD8504G, ESD8006 |

## PACKAGE DIMENSIONS

**UDFN10 2.5x1, 0.5P**
CASE 517BB
ISSUE O

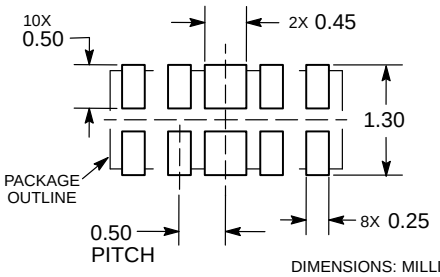



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.15 | 0.25 |
| b2 | 0.35 | 0.45 |
| D | 2.50 BSC | |
| E | 1.00 BSC | |
| e | 0.50 BSC | |
| L | 0.30 | 0.40 |
| L1 | --- | 0.05 |

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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