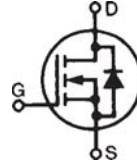


# Depletion Mode MOSFET

## IXTT16N10D2 IXTH16N10D2

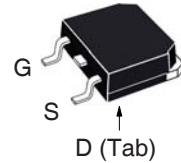
$V_{DSX} = 100V$   
 $I_{D(on)} \geq 16A$   
 $R_{DS(on)} \leq 64m\Omega$

N-Channel

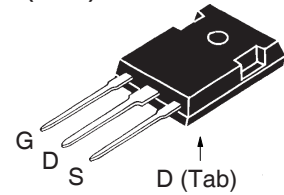


Symbol	Test Conditions	Maximum Ratings	
$V_{DSX}$	$T_J = 25^\circ C$ to $175^\circ C$	100	V
$V_{DGX}$	$T_J = 25^\circ C$ to $175^\circ C$ , $R_{GS} = 1M\Omega$	100	V
$V_{GSX}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$P_D$	$T_C = 25^\circ C$	830	W
$T_J$		- 55 ... +175	$^\circ C$
$T_{JM}$		175	$^\circ C$
$T_{stg}$		- 55 ... +175	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ C$
$T_{SOLD}$	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
$M_d$	Mounting Torque (TO-247)	1.13 / 10	Nm/lb.in
Weight	TO-268	4	g
	TO-247	6	g

TO-268 (IXTT)



TO-247 (IXTH)



G = Gate      D = Drain  
 S = Source    Tab = Drain

Symbol	Test Conditions ( $T_J = 25^\circ C$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSX}$	$V_{GS} = -5V$ , $I_D = 250\mu A$	100		V
$V_{GS(off)}$	$V_{DS} = 25V$ , $I_D = 4mA$	- 2.0		V
$I_{GSX}$	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			$\pm 100$ nA
$I_{DSX(off)}$	$V_{DS} = V_{DSX}$ , $V_{GS} = -5V$ $T_J = 150^\circ C$			5 $\mu A$ 250 $\mu A$
$R_{DS(on)}$	$V_{GS} = 0V$ , $I_D = 8A$ , Note 1			64 m $\Omega$
$I_{D(on)}$	$V_{GS} = 0V$ , $V_{DS} = 25V$ , Note 1	16		A

### Features

- Normally ON Mode
- International Standard Packages
- Molding Epoxies Meet UL94 V-0 Flammability Classification

### Advantages

- Easy to Mount
- Space Savings
- High Power Density

### Applications

- Audio Amplifiers
- Start-up Circuits
- Protection Circuits
- Ramp Generators
- Current Regulators
- Active Loads

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 20\text{V}$ , $I_D = 8\text{A}$ , Note 1	7	11	S
$C_{iss}$	$V_{GS} = -10\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		5700	pF
$C_{oss}$			1980	pF
$C_{rss}$			940	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = \pm 5\text{V}$ , $V_{DS} = 50\text{V}$ , $I_D = 8\text{A}$ $R_G = 3.3\Omega$ (External)		45	ns
$t_r$			43	ns
$t_{d(off)}$			340	ns
$t_f$			70	ns
$Q_{g(on)}$	$V_{GS} = \pm 5\text{V}$ , $V_{DS} = 50\text{V}$ , $I_D = 8\text{A}$		225	nC
$Q_{gs}$			22	nC
$Q_{gd}$			126	nC
$R_{thJC}$	TO-247			0.18 $^\circ\text{C/W}$
$R_{thCS}$			0.21	$^\circ\text{C/W}$

### Safe-Operating-Area Specification

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
SOA	$V_{DS} = 100\text{V}$ , $I_D = 5.6\text{A}$ , $T_C = 75^\circ\text{C}$ , $t_p = 5\text{s}$	556		W

### Source-Drain Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$V_{SD}$	$I_F = 16\text{A}$ , $V_{GS} = -10\text{V}$ , Note 1		0.80	1.30 V
$t_{rr}$	$I_F = 8\text{A}$ , $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$ , $V_{GS} = -10\text{V}$		205	ns
$I_{RM}$			8.50	A
$Q_{RM}$			0.88	$\mu\text{C}$

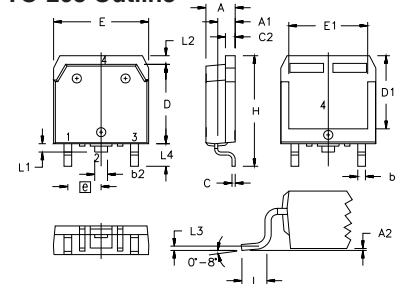
Note 1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

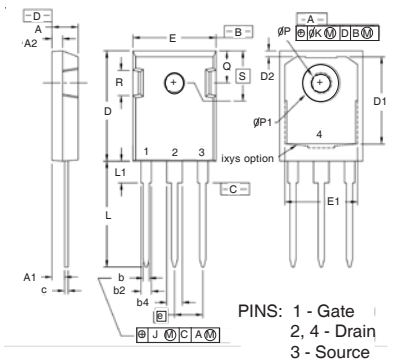
### TO-268 Outline



Terminals: 1 - Gate, 2,4 - Drain, 3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

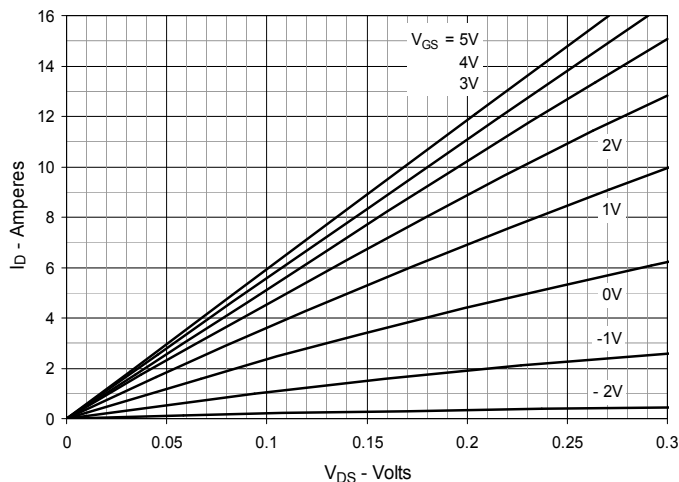
### TO-247 Outline



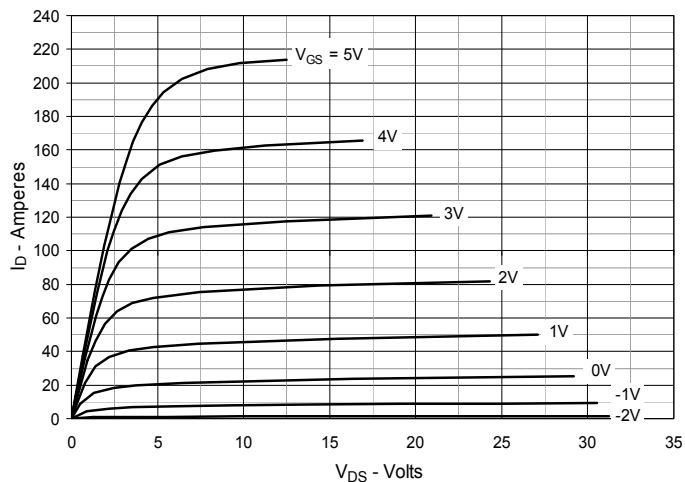
PINS: 1 - Gate, 2, 4 - Drain, 3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.545	.565	13.84	14.35
e	.215 BSC		5.45 BSC	
J	--	.010	--	0.25
K	--	.025	--	0.64
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
øP	.140	.144	3.55	3.65
øP1	.275	.290	6.99	7.37
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.242 BSC		6.15 BSC	

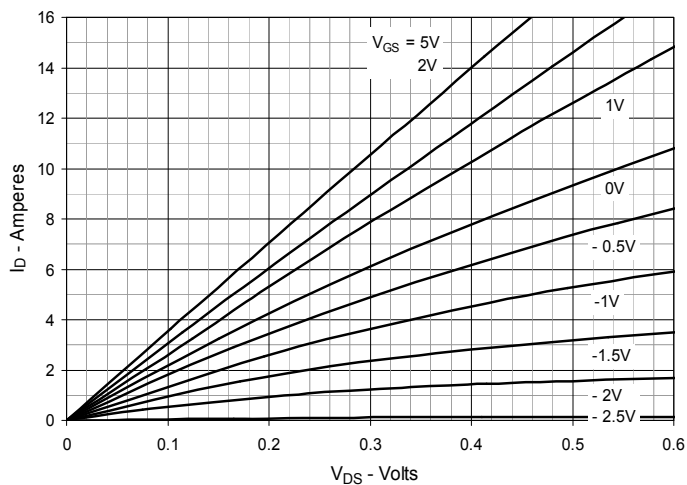
**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$**



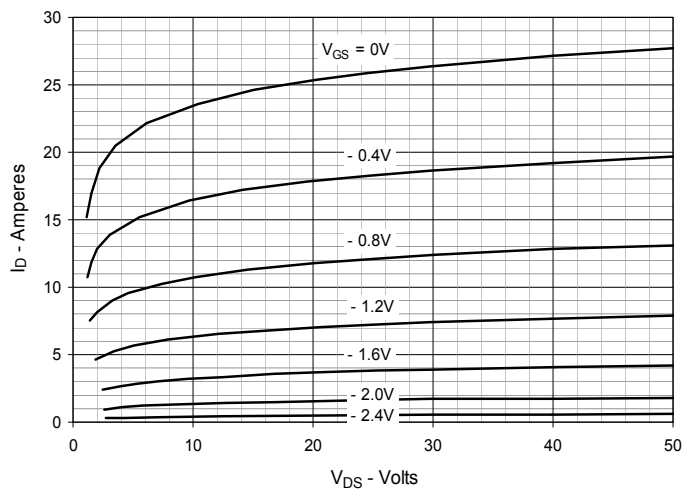
**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$**



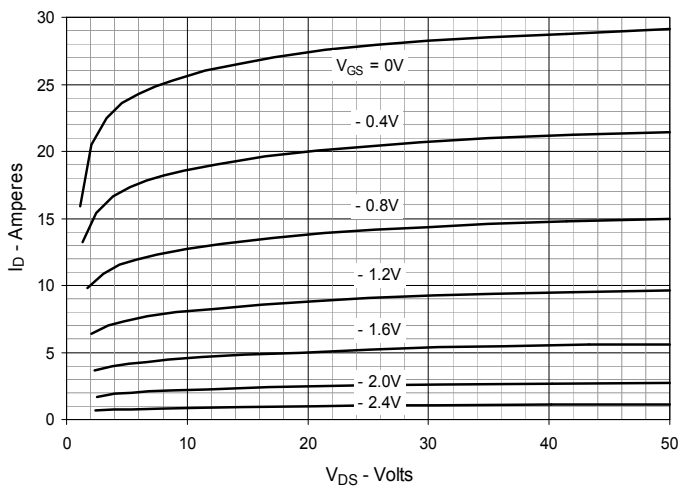
**Fig. 3. Output Characteristics @  $T_J = 150^\circ\text{C}$**



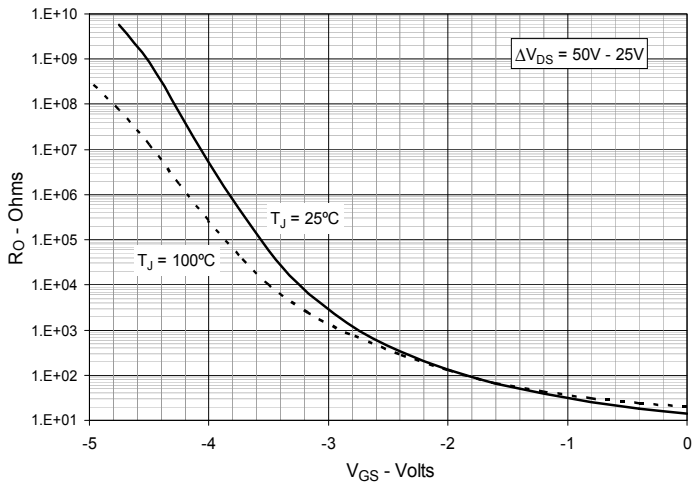
**Fig. 4. Drain Current @  $T_J = 25^\circ\text{C}$**



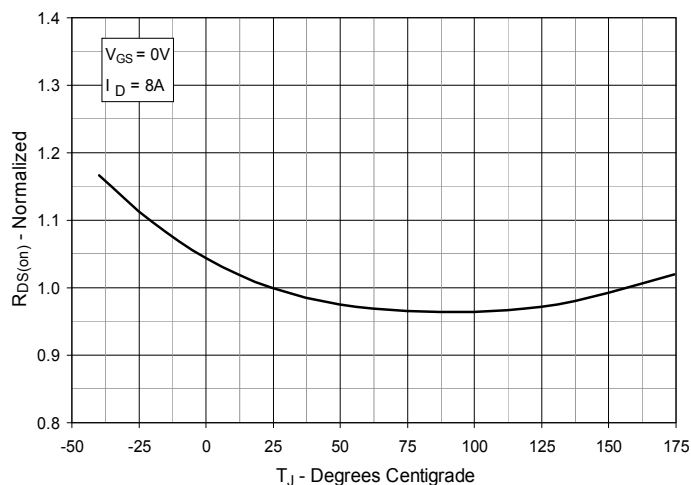
**Fig. 5. Drain Current @  $T_J = 100^\circ\text{C}$**



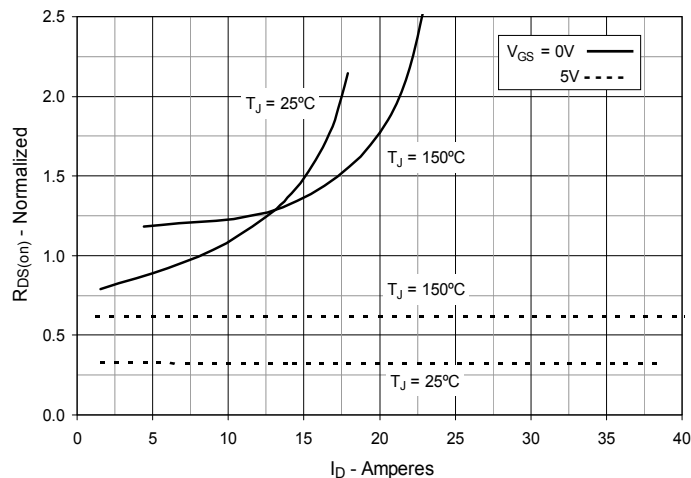
**Fig. 6. Dynamic Resistance vs. Gate Voltage**



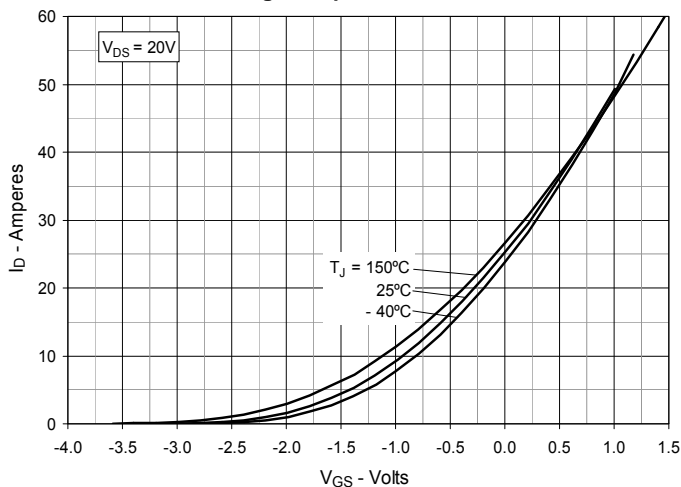
**Fig. 7. Normalized  $R_{DS(on)}$  vs. Junction Temperature**



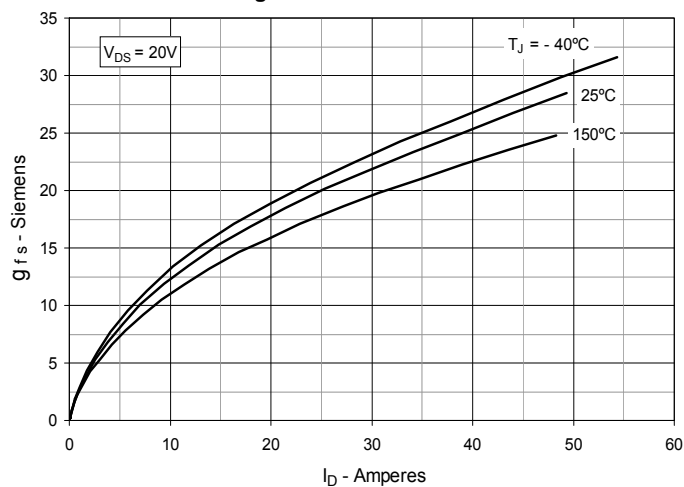
**Fig. 8.  $R_{DS(on)}$  Normalized to  $I_D = 8A$  Value vs. Drain Current**



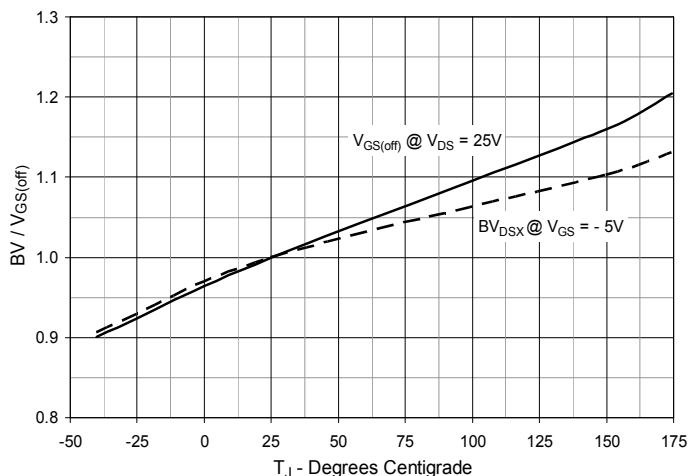
**Fig. 9. Input Admittance**



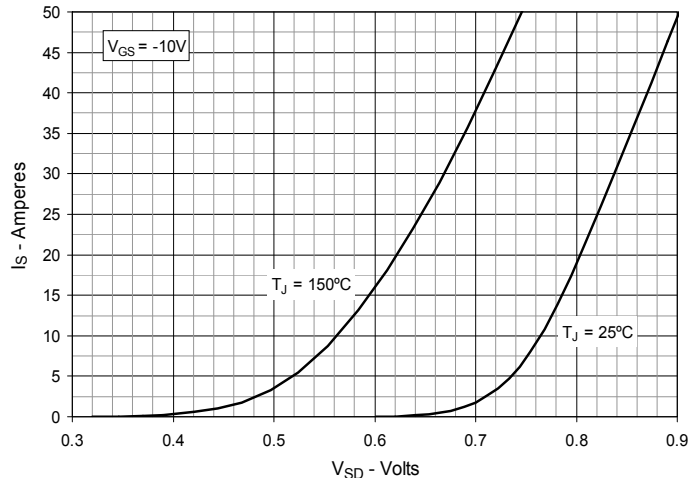
**Fig. 10. Transconductance**



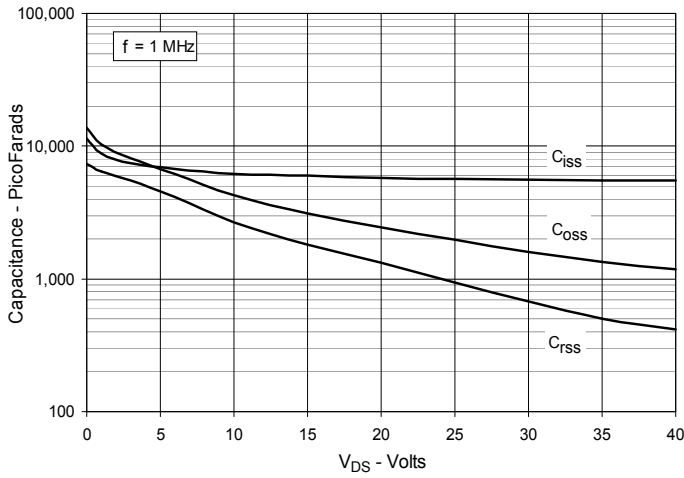
**Fig. 11. Normalized Breakdown and Threshold Voltages vs. Junction Temperature**



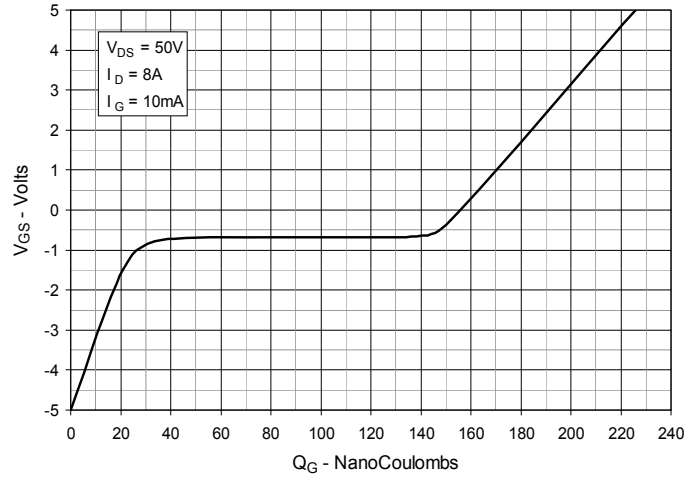
**Fig. 12. Forward Voltage Drop of Intrinsic Diode**



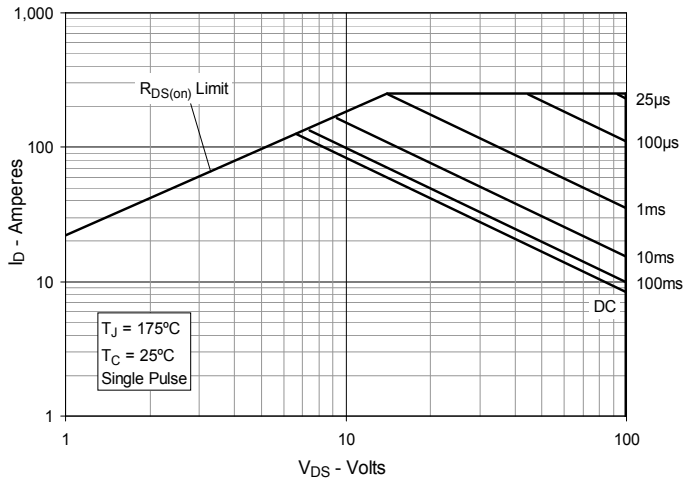
**Fig. 13. Capacitance**



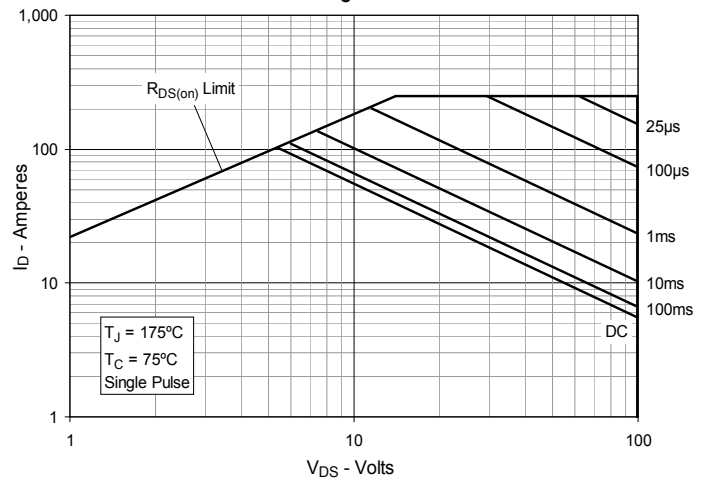
**Fig. 14. Gate Charge**



**Fig. 15. Forward-Bias Safe Operating Area @  $T_C = 25^\circ\text{C}$**



**Fig. 16. Forward-Bias Safe Operating Area @  $T_C = 75^\circ\text{C}$**



**Fig. 17. Maximum Transient Thermal Impedance**

