Issue No. :		ERTJ06073105
Date of Issue	:	July 31.2006
Classification	:	■ New □ Changed

PRODUCT SPECIFICATION FOR APPROVAL

Product Description	:	Multilayer Chip NTC Thermistors
Product Part Number	•	ERTJ0ER104J
		[EIA:0402]

.....

.....

Customers Part Number	:	
Country of Origin	:	Japan
Applications	:	Consumer Type Electric Equipment

XIf you approve this specification, please fill in and sign the below and return 1 copy to us.

Approval No	:		
Approval Date	:		
Excecuted by	:		
		(signature)	
Title	:		
Dept.	:		

	Prepared by : Engineering Section	
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If there is a question, please ask the engineering se	ction about it directly. Panasor	nic

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CLASSIFICATION	SPECIF	ICATIONS			No. 151S-E	RTJ-KE52E
SUBJECT	Multilaver Chip	NTC Thermistors			PAGE	l of 1
In	dividual Specificat				DATE	I 31, 2006
			、 ,			101, 2000
 Scope This specification appl Style and Dimensions 	lies to Multilayer Chip I	NTC Thermistors , siz	e 0402(EIA).			
	1			Table 1		
<		\leftarrow	Sym	ool Dimens	ions(mm)	
	L1		L	1.0 -	⊧/- 0.1	
			W	0.50 -	⊦/- 0.05	
			Т	0.50 -	+/- 0.05	
	L2		L1,I	.2 0.25 -	+/- 0.15	
<u>(</u>		<u>(</u>)				
3. Operating Temperatur - 40 to 125 °		nperature Range				
4 Evaluation of Dart N	umboro					
4. Explanation of Part Nu <u>E R T J</u>	umbers <u>0 </u>	<u>R 1</u>) 4	.1		
Common Code		B Value Non	ninal			
		Class Resis Code	tance	Resistance To	l Code	
		oode	-		erance - 5 %	
Size Code Code Size	ך ך		l	<u> Ј</u> т/	5 /0	
0 EIA:0402		g Style Code				
		Packagir 180Reel, Paper Tapin		/reel		
5. Individual Specificatio			g,			
Table 2						
Part Number	Rated Zero-power	B Value	Rated Maxir		Dissipation	Factor *3)
r art Number	Resistance *1)	(B _{25/50})	Dissipa	tion * ²⁾	(Reference	e value)
ERTJ0ER104J	100 kΩ +/- 5 %	4250 K +/- 2 %	66 r	nW	Approx. 2 r	mW / °C
ambient te	er Resistance : The v. mperature, 25.0°C +/- neration of heat is negli	0.1°C, under condit	ions such tha			
	Power Dissipation : Th				sed power dissipat	ion curve
	which can be continuo mbient temperature, 25		ermistor at	001 ratio (%)	Rated Maxi Pow er Diss	
† The maximun	n value of the pow	er dissipation which	can be			
	applied to the thermis tion") is equal to the rate		maximum lissipation	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		1
when the amb	pient temperature is le	ss than 25°C, and w	hen more	50 <u>50</u>		
than 25°C, it is	s based on the decreas	sed power dissipation	curve.	Max. F		
	r : The factor which inc		lied to the	25 0 L	25	125
by 1°C due	when the temperature to its self-heat dissipa	tion.	L		Temp. (deg.C)	-
† The dissipation	factor is a reference va	alue when mounted or	n a glass epox	y board (1.6	mmT).	
Note ;						
				APPROVAL	CHECK	DESIGN
Pan	asonic Electronic De	vices Co., Ltd.				
				Y. Sakaguti	T. Kawamura	T. Shinriki

CLASSIFICATION	SPECIFICATIONS	No. 151S-ERTJ-SG07E
SUBJECT	Multilayer Chip NTC Thermistors Common Specification for Standard Type	PAGE <u>1 of 5</u> DATE May 12, 2006
materials use (2) PBB and PB (3) All the materi Manufacture (4) This product	nd regulations epleting substances listed in the Montreal Protocol are not used in the ma of in this product. DE are intentionally excluded from materials used in this product. als used in this product are registered materials under the Law Concerni and Handling of Chemical Substances. complies with the RoHS, DIRECTIVE 2002/95/EC on the Restriction of t and electronic equipment.	ng Examination and Regulation of

(5) This product is subject to export procedures under export related laws and regulations such as the Foreign Exchange and Foreign Trade Law.

1-2. Limitation in Applications

This product was designed and manufactured for general-purpose electronic equipment such as household, office, information & communication equipment. When the following applications, which are required higher reliability and safety because the trouble or malfunction of this product may threaten the lives and/or properties, are examined, separate specifications suitable for the application should be exchanged.

Aerospace / Aircraft equipment, Warning / Antitheft equipment, Medical equipment, Transport equipment (Motor vehicles, Trains, Ship and Vessel), Highly public information processing equipment, Others equivalent to the above.

1-3. Production factory

- (1) Panasonic Electronic Devices Hokkaido Co., Ltd.
- (2) Panasonic Electronic Devices (Tianjin) Co., Ltd. (PEDTJ)

2. Scope

This specification applies to common specification for Multilayer Chip NTC Thermistors. If there is a difference between this common specification and any individual specifications, priority shall be given to the individual specifications.

2-1. This product shall be used for general-purpose electronic equipment such as audio/visual, home, office, information & communication equipment.

Depending on the application, the time frame for failure modes such as performance deterioration or the time in which short/open circuits may occur may be accelerated.

For products which require high safety levels, please carefully consider how a single malfunction can affect your product. Whenever any doubt about safety arises from this product, immediately inform us for technical consultation without fail, please.

2-2. This specification shall form a part of documents related with the agreement made and entered by and between your company and Matsushita Electric Industrial Co., Ltd.

3. Part Numb	er Code								
<u>ERTJ</u>	<u>1</u>	<u>V</u>	<u>A</u>	<u>101</u>	<u>J</u>	_			
(1)	(2)	<u>V</u> (3)	(4)	(5)	(6)	(7)			
2.4.Comm	an Cada (1)								
3-1.Comm	. ,								
ERIJ	: Multilayer Chip	NIC Them	nistors			C	Common Cod	е	
					Р	roduct Code		Type Code	
					ERT	NTC Thermistors	J Multil	ayer Chip Type	(SMD)
3- 2. Size Co	ode (2)								
Z : size	e 0201 / EIA								
0 : size	e 0402 / EIA								
1 : size	e 0603 / EIA								
Note ;.									
						A	PPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., L							Y. Sakaguti	T.Kawamura	S. Inagaki

CLASSIFICA	TION	SF	PECIFICATIO	NS				No. 151S-l	ERTJ-	SG07E	
SUBJECT		Multilaver	Chip NTC Thermistors						PAGE 2 of 5		
		Common Spe	•				-	DATE		12, 2006	
	in each	e Code (3) n Individual Specification					I		way	12, 2000	
3- 4. B Value (1										
Co	de	Center of B Value									
A		2701~2800K									
G		3301~3400K									
N		3801~3900K									
P		4001~4100K									
R		4201~4300K									
S		4301~4400K									
Т		4401~4500K									
V	/	4701~4800K									
	minal F two dig	Resistance is expressed gits represent significant				Syr	mbol (Ex.) 102 103 104	Nom	inal Res (ohm 1000 10000) 0	
3-6. Resistan	ice Tole	erance Code (6)					101		10000		
Shown	in eacł	n Individual Specification									
3-7. Special S											
A specif	ic code	e shall be given for identi	fication as individua	al specification or desi	ign rankin	ng if ne	ecessary.				
4. Operating Te Shown in ea		ature Range Jividual Specification									
5 Coldoring m	othod										
5. Soldering m Soldering m		of the multilayer chip NT	C thermistor shall	be reflow soldering.							
-				C C							
6. Performance The perform		of the multilayer chip NT	°C thermistor and it	s test conditions shall	be specif	fied in	Table 2.				
to 75%.		specified, all tests and m are doubted, a further te								-	
		,,		· · · · · · · · · · · · · · · · · · ·							
8. Structure											
		Fig. 1				Table	1				
	-			(3)	1	No.		Name			
				(4)			Semicond		Ceram	ics	
ſ	$\angle \not$				-, _	(2)	Internal)	
						(3)		Substra Electro)	
						(4) 1		Interme		<u>)</u>	
))		· /		Electro)	
		(2)			((5)		Externa		、	
		(1)	\sim					Electro	ue (SN)	
		(1)									
Note ;											

CLAS	SIFICATION	SPECIFICATIONS		No. 151S-ERTJ-SG07E
SUBJI	ECT	Multilayer Chip NTC Thermistors		PAGE 3 of 5
	Co	ommon Specification for Standard Typ	De	DATE May 12, 200
		Table 2		•
No.	Test	Performance	Test Me	
1	Appearance	There shall be no defects which affect the life and use.	Check with a magnifying glas	S (3X)
2	Dimensions	Shown in each Individual Specification	Inspection with slide calipers projector	
3	Rated Zero-power Resistance (R ₂₅)	Shown in each Individual Specification	The value of the d.c. resistan the rated ambient temperal under the power less than 0. self heat generation.	ture of 25.0+/-0.1deg.C
4	B Value	Shown in each Individual Specification	The Zero-power resistances;	
		* Individual Specification shall specify B _{25/50} or B _{25/85} .	ured respectively at $T_1(\text{deg.C})$ The B value is calculated by t	
		01 025/85.	$\ln(R)$	$(1) - \ln(R_2)$
			$B_{T_1/T_2} = \frac{\ln(R)}{1/(T_1 + 273.12)}$	$(5) - 1/(T_2 + 273.15)$
			T_1	T ₂
			B _{25/50} 25.0+/-0.1°	
			B _{25/85} 25.0+/-0.1°	C 85.0+/-0.1°C
5	Adhesion	The terminal electrode shall be free from peeling or signs of peeling.	Specimens shall be soldered shown in Fig.2, and the follo the arrow direction for 10 second •Force EIA size 0201 : 2N others size : 5N	owing force is applied in onds.
		EIA size 0201, 0402	EIA size 0603	
		Gampre	* Pard Unit:mm project of the second seco	Sample
6	Bending Strength	There shall be no cracks and other mechani- cal damage.	After soldering a specimen of Fig.3), 1mm of bending shall	n the substrate (shown in
		Change of Zero-power Resistance (R ₂₅) : Within +/-5%	Bending speed : 1mm/s	Bendi
		(to be continued)		

CLASSIFICATION	
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SUBJECT

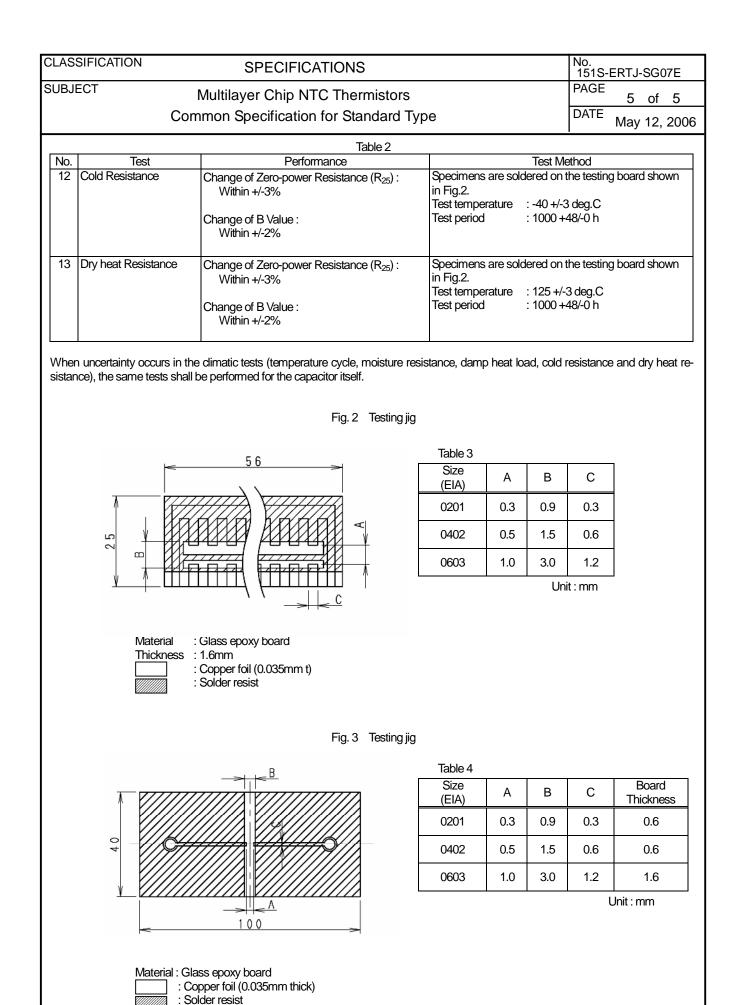
SPECIFICATIONS

No. 151S-I PAGE	ERTJ-	SG)7E
PAGE	4	of	_
DATE	May	12	200

Multilayer Chip NTC Thermistors

Common Specification for Standard Type

ю.	Test	Performance			Test Meth	
7	Resistance to soldering heat	There shall be no cracks and other mechanica damage. Change of Zero-power Resistance (R ₂₅) : Within +/-3% Change of B Value : Within +/-2%	Dippin Speci minal Precc Solde Flux:	ng perio mens s electroc onditionii Step 1 2 er : H63/ Concer	d : 3.0 +/-0.5 hall be dipped in des are completely ng : Heat treatmer (deg.C) 80 to 100 150 to 200	s solder so that both y immersed. nt Period (s) 120 to 180 120 to 180 % by weight of Ros
8	Solderability	More than 75% of the soldered area of both terminal electrodes shall be covered with fresh solder.	Dippin A spe trodes Solde Flux:	ng perio cimen s s are co er : H63/ Concer	d : 4 +/- 1 s shall be dipped so mpletely immerse A(JIS-Z-3282) stration about 256 5902) ethanol solu	b that both terminal el d. % by weight of Ros ttion
9	Temperature Cycling	Change of Zero-power Resistance (R ₂₅) : Within +/-3% Change of B Value : Within +/-2%	Specimens shall be soldered on the testing jig sl in Fig. 2. The specimens are conditioned to be each tem ture from step 1 to 4 in this order for the period sl in the table below. Regarding this conditioning as one cycle, 100 cycles shall be continuously performed.		d to be each tempera er for the period show one cycle,	
			Ste	ер	Temperature(°C)	Period(min)
					-40 +/- 3	30 +/- 3
					Room temperature	
			2		125 +/- 5 Room temperature	30 +/- 3 e 3 max.
10	Moisture Resistance	Change of Zero-power Resistance (R ₂₅) : Within +/-3% Change of B Value : Within +/-2%	show Test t	n in Fig.: emperat ive hum	2. ture : 85 +/-2 de	•
11	Damp Heat Load	Change of Zero-power Resistance (R ₂₅) : Within +/-3% Change of B Value : Within +/-2%	show Test t Relat	n in Fig. emperative hum ed powe	2. ture : 85 +/-2 de idity : 85 +/-5 %	D.C.)
		(to be continued)				



Note;

CLASSIFICATION SPECIFICATIONS	No. 151S-	ERTJ-S	S03E
SUBJECT Multilayer Chip NTC Thermistors	PAGE	1 of	
Common Specification (Precautions for Use)	DATE N	/lay 12,	
 Precautions for Use Multilayer Chip NTC Thermistors (hereafter referred to as "Thermistors") may fail in a sho open circuit mode, when subjected to severe conditions of electrical environmental an beyond the specified "Rating" and specified "Conditions" in the Specification, resulting glowing in the worst case. The following "Precautions for Safety" and "Application Notes major consideration for use. 	ort circuit n nd/or mech g in burnou	mode or nanical ut, flami	r in an stress ing or
 2. Operating Conditions and Circuit Design 2. 1.Circuit Design 2-1-1. Operating Temperature and Storage Temperature The specified "Operating Temperature Range" in the Specifications is the absolute n temperature rating. Every circuit mounting a Thermistor shall be operated within th Temperature Range". The Thermistors mounted on PCB shall be stored without opera "Storage Temperature Range" in the Specifications. 	he specifie	ed "Ope	erating
 2-1-2. Operating Power Thermistors shall not be operated in excess of the "Maximum power dissipation". If the Thermistors are operated beyond the specified Maximum power dissipation, it may damage due to thermal run away. For temperature detection applications, the accuracy may be greatly influenced by s the heat dissipation of the Thermistor, even if the Thermistor is operated under the specification. Check safety and reliability in your circuit. 	self-heat ge	eneratio	on and
 The Maximum power that can be continuously applied under static air at a certain ambient temperature. The Maximum power dissipation under ambient temperature 25°C or less is the same with the rated maximum power dissipation, and Maximum power dissipation beyond 25°C depends on the right Decreased power dissipation curve. [Dissipation factor] The constant amount power required to raise the temperature of the Thermister 1°C through self heat generation under stable temperatures. 	d power dissipat	kimum	
 2-1-3. Environmental Restrictions The Thermistors shall not be operated and/or stored under the following conditions. (1) Environmental conditions (a) Under direct exposure to water or salt water (b) Under conditions where water can condense and/or dew can form (c) Under conditions containing corrosive gases such as hydrogen sulfide, sulfur ammonia (2) Mechanical conditions Under severe conditions of extreme vibrations or shocks. 2-1-4. Measurement of Resistance The resistance of the Thermistors varies dependent on ambient temperatures and following points when measuring resistance values of the Thermistors during inspectit them for circuits. (1) Measurement temp : 25±0.1°C Measurement in liquid (silicon oil) is recommended for a stable measurement tem (2) Power : 0.10 mW max. 4 terminal measurement with a constant-current power supply is recommended. 	d self-heati ion or whei	ing. Not	te the
Note :			
Panasonic Electronic Devices Co. 1 td	CHECK F.Kawamura	DESIC	GN nagaki

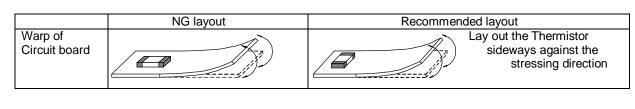
CLASSIFICATION SPECIFICATIONS No. 151S-ERTJ-SS03E							S03E	
SUBJECT M	ultilayer Chip NTC	Thermis	tors			PAGE	2 of	7
Commo	on Specification (Pre	caution	s for U	se)		DATE	May 12,	2006
 2- 2.Design of Printed Circuit Board 2-2-1. Selection of Printed Circuit Boards When the Thermistors are mounted and soldered on an "Alumina Substrate", the substrate influences the Thermistors' reliability against "Temperature Cycles" and "Heat shock" due to the difference in the thermal expansion coefficient between them. Confirm that the actual board used does not deteriorate the characteristics of the Thermistors. 2-2-2. Design of Land Pattern (1) Recommended land dimensions are shown below for proper amount of solder to prevent cracking at the time of excessive stress to the Thermistors due to increased amount of solder. 								
[Recommended lanc Land	d dimensions (Ex.)]						Unit: r	nm
	Size Code (EIA)		Compone Dimensio W		а	b	С	
$ \downarrow $	<u>Z (0201)</u>	0.6	0.3	0.3	0.2 to 0.3	0.25 to 0.3	0.2 to	
b a	Solder 0 (0402) resist 1 (0603)	1.0	0.5	0.5 0.8	0.4 to 0.5 0.8 to 1.0	0.4 to 0.5 0.6 to 0.8	0.4 to 0.6 to	
solder on the righ	shall be designed to ha t land is different from th ger amount of solder so <u>Recomme</u>	hat on the lidifies lat	e left land er during	, the cor g cooling	nponent may			
	essive amount (b) of solder	Proper a of sold	imount er sold) Insufficient a of solder			
PC boards. (1) Solder resist shall (2) Solder resist shall ·Component ·The Thermi	Ider resist is effective in I be utilized to equalize to I be used to divide the p ts are arranged closely. Istor is mounted near a char stor is placed near a char ow.	he amou attern for	nts of sol the follo	der on b wing cas	ooth sides. ses;	ng the amour	it of sola	er on
	NG Applications a	and Reco	mmende	d Applica	ations			
	NG applie	cations	minenae	Imp	proved applica	tions by patte	rn divisio	n
Mixed mounting with a component with lead wires					Solder resist	Sec	tional vie	2007
Arrangement near chassis	Chassis	d solder)	tional vie		Solder resist	Sec	tional vie	
Retro-fitting of component with lead wires	Soldering iron	Re co	wire of tro-fitted omponen tional vie		Solder resis	VA	tional vie	ew
Lateral arrangement	Land	Portio	n to be essively coldered				der resist	
Note ;								1

CLASSIFICATION	SPECIFICATIONS	No. 151S-ERTJ-SS03E
SUBJECT	Multilayer Chip NTC Thermistors	PAGE 3 of 7
	Common Specification (Precautions for Use)	DATE May 12, 2006

2-2-4. Component Layout

The Thermistors/components shall be placed on the PC board such that both electrodes are subjected to uniform stresses, or to position the component electrodes at right angles to the grid glove or bending line. This should be done to avoid cracking the Thermistors from bending the PC board after or during placing/mounting on the PC board.

(1) To minimize mechanical stress caused by warp or bending of a PC board, please follow the recommended Thermistor layout below.

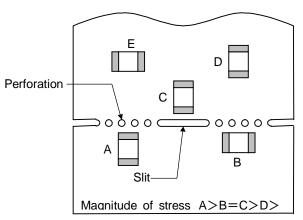


- (2) The following layout is for your reference since mechanical stress near the dividing/breaking position of a PC board varies depending on the mounting position of the Thermistors.
- (3) The magnitude of mechanical stress applied to the Thermistors when the circuit board is divided is in the order of push back < slit < V-groove < perforation.

Also take into account the layout of the Thermistors and the dividing/breaking method.

2-2-5. Mounting Density and Spaces

If components are arranged in too narrow a space, the components can be affected by solder bridges and solder balls. The space between components should be carefully determined.



3. Precautions for Assembly

3-1.Storage

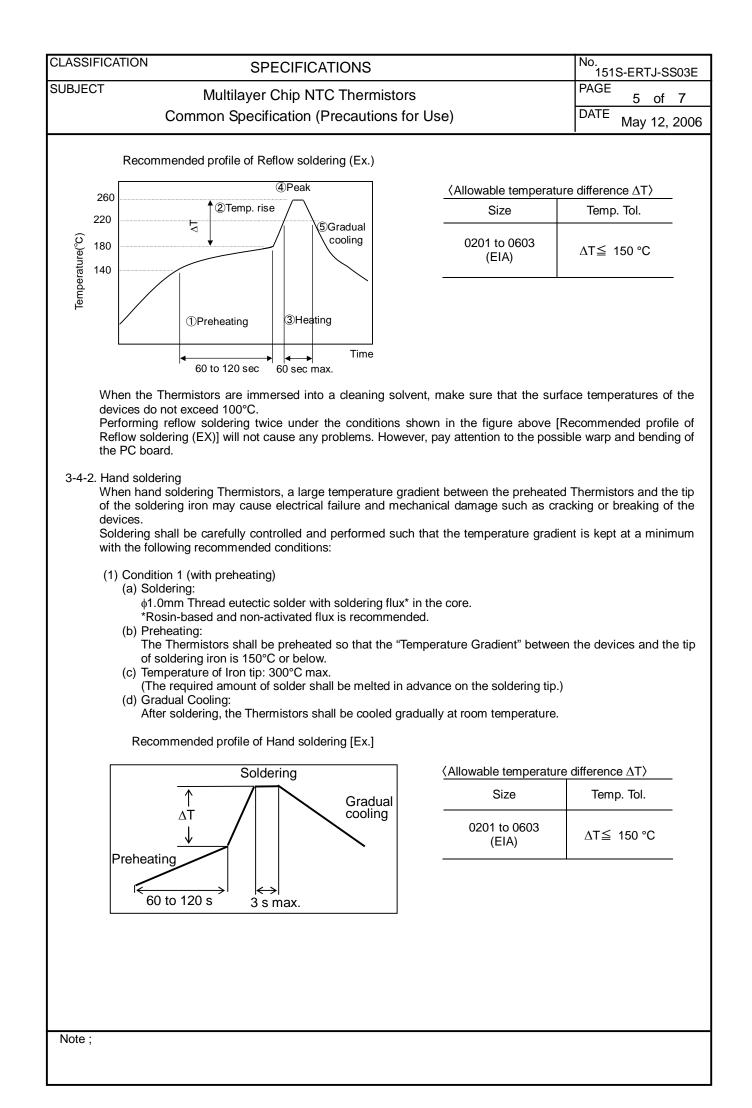
- (1) The Thermistors before mounting on PCB shall be stored between 5 40°C and 20 70% RH, not under severe conditions of high temperature and humidity.
- (2) If stored in a place that is humid, dusty, or contains corrosive gasses (hydrogen sulfide, sulfurous acid, hydrogen chloride and ammonia, etc.), the solderability of terminal electrodes may deteriorate. In addition, storage in a place subjected to heating and/or exposed to direct sunlight will cause deformed tapes
- and reels. This may also lead to components sticking to tapes. Both of which can result in mounting problems.(3) Do not store components longer than 6 months. Check the solderability of products that have been stored for more than 6 months before use.

3- 2. Chip Mounting Consideration

- (1) When mounting the Thermistors/components on a PC board, the Thermistor bodies shall be free from excessive impact loads such as mechanical impact or stress due to the positioning, pushing force and displacement of vacuum nozzles during mounting.
- (2) Maintenance and inspection of the Chip Mounter must be performed regularly.
- (3) If the bottom dead center of the vacuum nozzle is too low, the Thermistor will be cracked by excessive force during mounting.
 - The following precautions and recommendations are for your reference in use.
 - (a) Set and adjust the bottom dead center of the vacuum nozzles to the upper surface of the PC board after correcting the warp of the PC board.
 - (b) Set the pushing force of the vacuum nozzle during mounting to 1 to 3 N in static load.
 - (c) For double surface mounting, apply a supporting pin on the rear surface of the PC board to suppress the bending of the PC board in order to minimize the impact of the vacuum nozzles. Typical examples are shown in the following table.

Note ;

CLASSIF	ICATION	SPECIFICATIONS		No. 151S-ERTJ-SS03	
SUBJECT	Mul	tilayer Chip NTC Thermistors		PAGE 4 of 7	
	Common	Specification (Precautions for Use))	DATE May 12, 200	
				,,,	
		NG mounting	Recommend		
			The supporting pin does not necessarily have to be positioned beneath the Thermistor.		
		\simeq	P		
	Single surface	Crack		1	
	mounting				
			Supporting		
			pin	d	
		$\overset{\frown}{\simeq}$	2]	
		\square		1	
	Double surface				
	mounting				
		Separation⊸ / of solder Crack	Supporting	d	
			pin		
(4) - (5) 	The closing dimension positioning chucks shal mechanical impact durin Maximum stroke of the 0.5mm at 90mm span.	nozzles so that their bottom dead center du as of the positioning chucks shall be c I be performed regularly to prevent chipping positioning due to worn positioning chuc nozzle shall be adjusted so that the max The PC board shall be supported by an ade	ontrolled. Maintenance ng or cracking of the ks. imum bending of PC b	e and replacement of Thermistors caused b board does not excee	
(4) - (5) (5) (3- 3.Sele Solo use. (1) - (2) \ (3- 4.Solo 3-4.Solo 3-4-1.	The closing dimension positioning chucks shal mechanical impact durin Maximum stroke of the 0.5mm at 90mm span. ⁻ ection of Soldering Flux dering flux may serious The soldering flux shoul Do not use soldering flu When applying water-so on the surface of PC bo dering Reflow soldering In reflow soldering, the conduction system such System" (VPS)". Large temperature grad electrical failure and me	as of the positioning chucks shall be co I be performed regularly to prevent chipping positioning due to worn positioning chuc nozzle shall be adjusted so that the max The PC board shall be supported by an add add date a halogen based content of 0.1 wt. x with strong acid. Duble soldering flux, wash the Thermistors ards may deteriorate the insulation resistant e mounted Thermistors/Components are go in as an "Infrared radiation and hot blast so ients such as the rapid heating and cooling schanical damage to the devices. e soldering process be controlled by t	ontrolled. Maintenance ng or cracking of the ks. imum bending of PC k equate number of support ors. The following sha % (converted to chlorin sufficiently because the nee on the Thermistors' generally heated and oldering system" or a " g which occurs during the he following recommend	e and replacement of Thermistors caused by poard does not exceed orting pins. Ill be confirmed before he) or below. e soldering flux residue ' surface. soldered by a thermat Vapor Phase Soldering his process may cause ended conditions and	
(4) - (5) (5) (3- 3.Sele Solo use. (1) - (2) \ (3- 4.Solo 3- 4.Solo 3-4-1.	The closing dimension positioning chucks shal mechanical impact durin Maximum stroke of the 0.5mm at 90mm span. T ection of Soldering Flux dering flux may serious The soldering flux shoul Do not use soldering flu When applying water-so on the surface of PC bo dering Reflow soldering In reflow soldering In reflow soldering, the conduction system such System" (VPS)". Large temperature grad electrical failure and me It is essential that th precautions.	as of the positioning chucks shall be can be performed regularly to prevent chipping positioning due to worn positioning chuc nozzle shall be adjusted so that the max The PC board shall be supported by an add duy affect the performance of the Thermist d have a halogen based content of 0.1 wt. x with strong acid. Duble soldering flux, wash the Thermistors ards may deteriorate the insulation resistar e mounted Thermistors/Components are go in as an "Infrared radiation and hot blast so itents such as the rapid heating and cooling inchanical damage to the devices. e soldering process be controlled by t <u>Temperature</u>	ontrolled. Maintenance ng or cracking of the ks. imum bending of PC k equate number of supp ors. The following sha % (converted to chlorin sufficiently because the nce on the Thermistors generally heated and oldering system" or a " g which occurs during t he following recommendation Period or Sp	e and replacement of Thermistors caused by board does not exceed orting pins. Ill be confirmed before he) or below. e soldering flux residue ' surface. soldered by a therma Vapor Phase Soldering his process may cause ended conditions and eed	
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CLASSIFICATION	SPECIFICATIONS		No. 151S-ERTJ-SS03E		
SUBJECT	Multilayer Chip NTC Thermistors	PAGE 6 of 7			
	Common Specification (Precautions fo	or Use)	DATE May 12, 2006		
	 (a) Soldering iron tip shall never directly touch the ceramic dielectrics and terminal electron Thermistors. (b) The lands are sufficiently preheated with a soldering iron tip before sliding the soldering iron terminal electrodes of the Thermistor for soldering. Conditions of Hand soldering without preheating 				
(b) Th	he lands are sufficiently preheated with a solderi rminal electrodes of the Thermistor for soldering.		soldering iron tip to the		
(b) Th	he lands are sufficiently preheated with a solderi rminal electrodes of the Thermistor for soldering.		soldering iron tip to the		
(b) Th	he lands are sufficiently preheated with a solderi rminal electrodes of the Thermistor for soldering.	without preheating	soldering iron tip to the		
(b) Th	he lands are sufficiently preheated with a solderi rminal electrodes of the Thermistor for soldering. Conditions of Hand soldering v	without preheating Condition	soldering iron tip to the		
(b) Th	Temperature of Iron tip	without preheating Condition 270 °C Max.	soldering iron tip to the		

3- 5.Post Soldering Cleaning

3-5-1. Cleaning solvent

Soldering flux residue may remain on the PC board if cleaned with an inappropriate solvent. This may deteriorate the electrical characteristics and reliability of the Thermistors.

3-5-2. Cleaning conditions

Inappropriate cleaning conditions such as insufficient cleaning or excessive cleaning may impair the electrical characteristics and reliability of the Thermistors.

- (1) Insufficient cleaning can lead to:
 - (a) The halogen substance in the residue of the soldering flux may cause the metal of terminal electrodes to corrode.
 - (b) The halogen substance in the residue of the soldering flux on the surface of the Thermistors may change resistance values.
 - (c) Water-soluble soldering flux may have more remarkable tendencies of (a) and (b) above compared to those of rosin soldering flux.
- (2) Excessive cleaning can lead to:
 - (a) Overuse of ultrasonic cleaning may deteriorate the strength of the terminal electrodes or cause cracking in the solder and/or ceramic bodies of the Thermistors due to vibration of the PC boards.
 - Please follow these conditions for Ultrasonic cleaning: Ultrasonic wave output : 20 W/L max.
 - Ultrasonic wave frequency : 40 kHz max.
 - Ultrasonic wave cleaning time : 5 min. max.

3-5-3. Contamination of Cleaning solvent

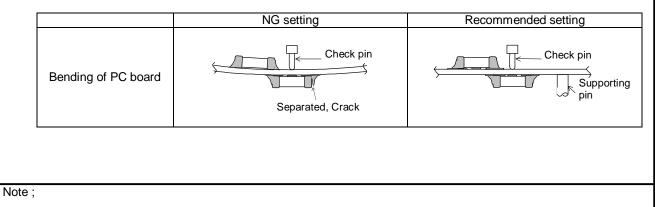
Cleaning with contaminated cleaning solvent may cause the same results as insufficient cleaning due to the high density of liberated halogen.

3- 6.Inspection Process

When mounted PC boards are inspected with measuring terminal pins, abnormal and excess mechanical stress shall not be applied to the PC board or mounted components, to prevent failure or damage to the devices.

(1) Mounted PC boards shall be supported by an adequate number of supporting pins with bend settings of 90 mm span 0.5mm max.

(2) Confirm that the measuring pins have the right tip shape, are equal in height and are set in the correct positions. The following figures are for your reference to avoid bending the PC board.



CLASSIFICATION	SPE	CIFICATIONS		No. 151S-ERTJ-SS03E
SUBJECT	Multilayer Cl	nip NTC Thermistors		PAGE 7 of 7
	Common Specifica	ation (Precautions for Use)		DATE May 12, 2006
against moistur Thermistors in t (1) Do not use	ace of a PC board on re and dust, it shall be the actual equipment. coating materials that a coating materials with	which the Thermistors have been confirmed that the protective coatin are corrosive or chemically active. large thermal expansivity to prever	ig does not influen	d with resin to protect ce the reliability of the
shown belo	and excessive mechar w can cause cracking in		rsion	Bending
speed by us from mecha	sing a jig or apparatus t nical damage.	ds shall be done carefully at mode to prevent the Thermistors on the bo		Torsion
The outline It is recommoccur, this v	vay there will be no con I the PC board at a po		onents or Thermist	tors on the PC board.
Outlin	ne of Jig	NG dividing	Recommer	nded dividing
PC board	V-groove PC board splitting jig	Load direction Load position PC board V-groove	PC board	
The Thermi if dropped. Never use impaired an (2) When hand the Thermis When mour between the or cracking	stors shall be free from stor body is made of ce a Thermistor which h d failure rate increased ling PC boards with Th tors to collide with anon ted PC boards are har e corner of a PC board	ermistors mounted on them, do not a	y be allow npact nage	Floor Mounted PCB
	autions described abov ting conditions, please			
Note ;				

CLASSFICATION	SPECIFICATIONS	No. 151S-ERTJ-SV02E
SUBJECT	Multilayer Chip NTC Thermistors Taped and Reeled Packaging Specifications	PAGE 1 of 4 DATE May 12, 2006
2. Applicable Standa EIAJ (Electric Inc	n applies to taped and reeled packing for Multilayer chip NTC Thermist ards dustries Association of Japan) Standard EIAJ RC-1009B Industrial Standard) Standard JIS C 0806	tors.
 Packing Specifica 1.Structure and Paper taping 		

- 1) Carrier tape : Shown in Fig. 4., Fig5.
- 2) Reel : Shown in Fig.6.
- 3) Packaging : We shall pack suitably in order prevent damage during transportation or storage.

3-2.Packing Quantity

Size(EIA)	Quantity (pcs./reel)	
0201	15000	
0402	10000	
0603	4000	

3-3.Marking on the Reel

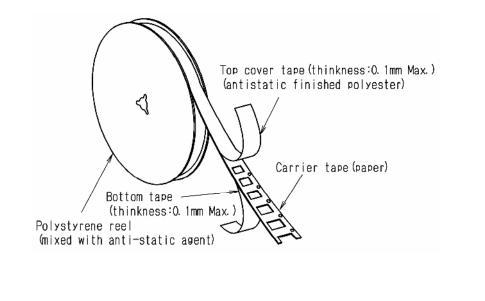
The following items are described in the side of a reel in English at least.

- 1) Part Number
- 2) Quantity
- 3) Lot Number
- 4) Place of origin

3-4.Structure of Taping

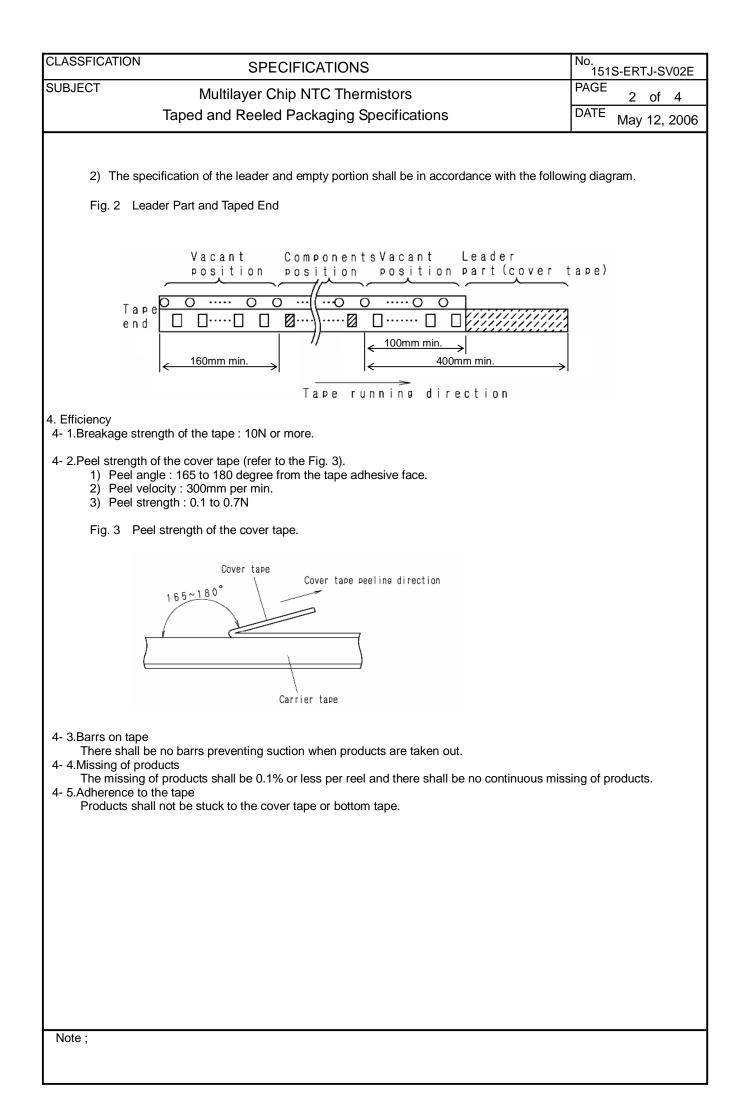
1) The direction of winding of taping on the reel shall be in accordance with the following diagram.

Fig. 1 Paper Taping

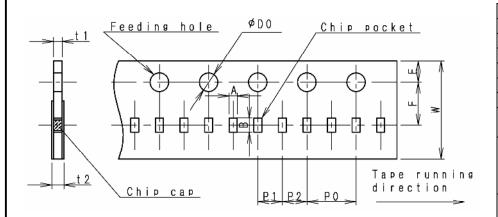


Note :

	APPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	S. Inagaki



CLASSFICATIO	N SPECIFICATIONS	No. 151S-ERTJ-SV02E
SUBJECT	Multilayer Chip NTC Thermistors Taped and Reeled Packaging Specifications	PAGE <u>3 of 4</u> DATE May 12, 2006
Fig. 4	Carrier Tape Dimension (EIA 0201 and 0402)	

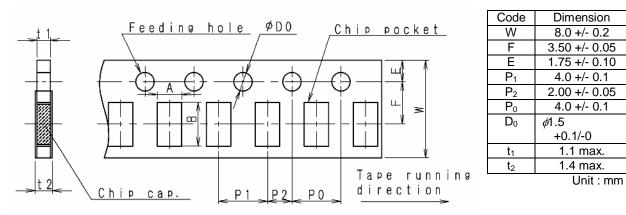


Code	Dimension		
W	8.0 +/- 0.2		
F	3.50 +/- 0.05		
E	1.75 +	/- 0.10	
P ₁	2.00 +	/- 0.05	
P ₂	2.00 +	/- 0.05	
P ₀	4.00 +	/- 0.05	
D_0	<i>ф</i> 1.5		
	+0.1/	-0	
t ₁	06	0.5	
	type	max.	
	10	0.7	
	type	max.	
t ₂	06	0.8	
	type	max.	
	10	1.0	
	type	max.	

Unit : mm

Size Code	EIA 0201	EIA 0402
A	0.37 +/- 0.03	0.62 +/- 0.05
В	0.67 +/- 0.05	1.12 +/- 0.05

Fig. 5 Carrier Tape Dimension (EIA 0603)



EIA 0603	
1.0 +/- 0.1	
1.8 +/- 0.1	

Note;

